

FIG. 1

FIG. 2 is a block diagram of a Processor Element (PE) 201. The PE 201 includes a PE Bus 223, a PU 203, a DMAC 205, and a series of APUs 207, 209, 211, 213, 215, 217, 219, and 221. The PE 201 is connected to a DRAM 225 via a bidirectional bus 227.

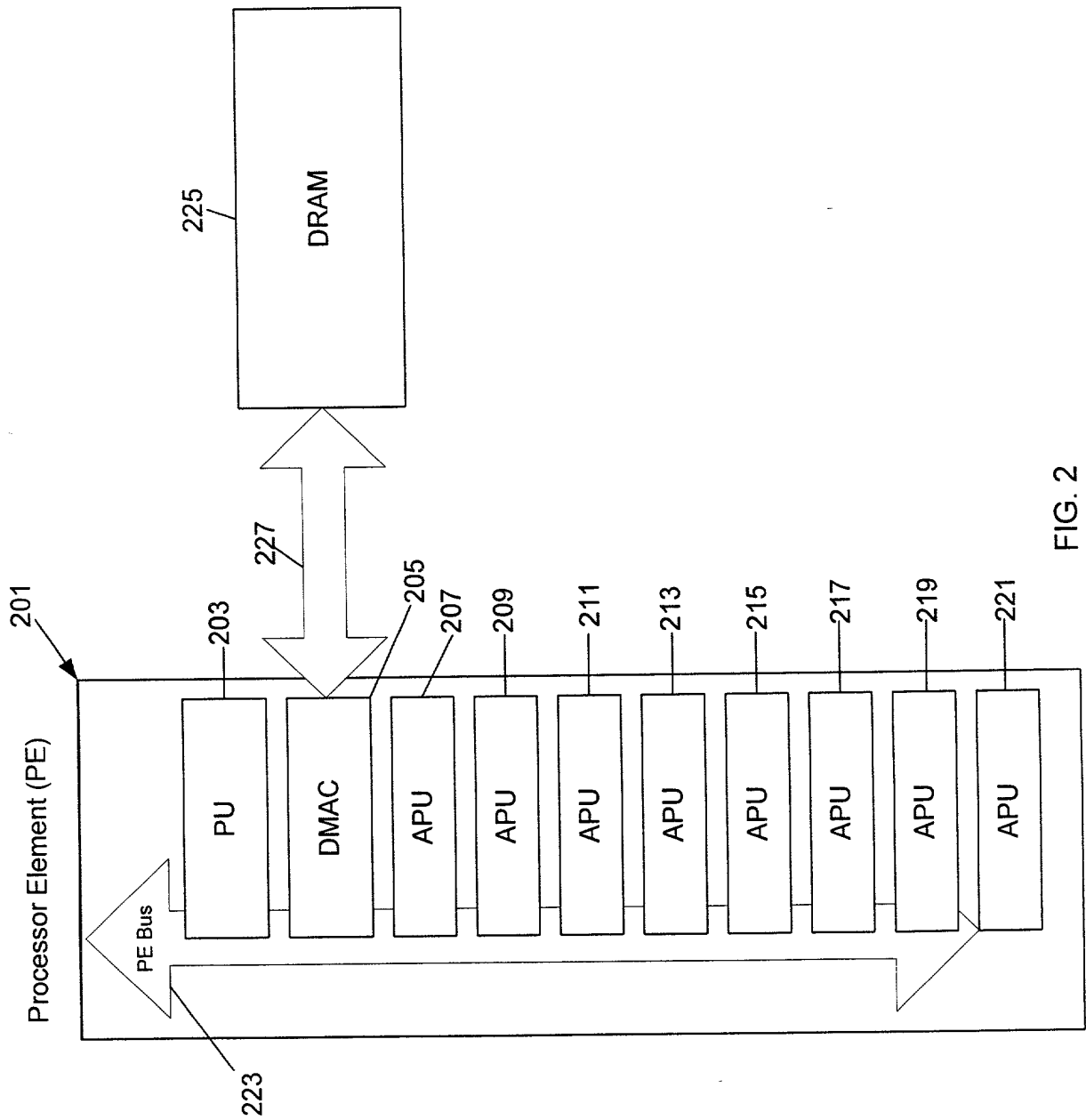


FIG. 2

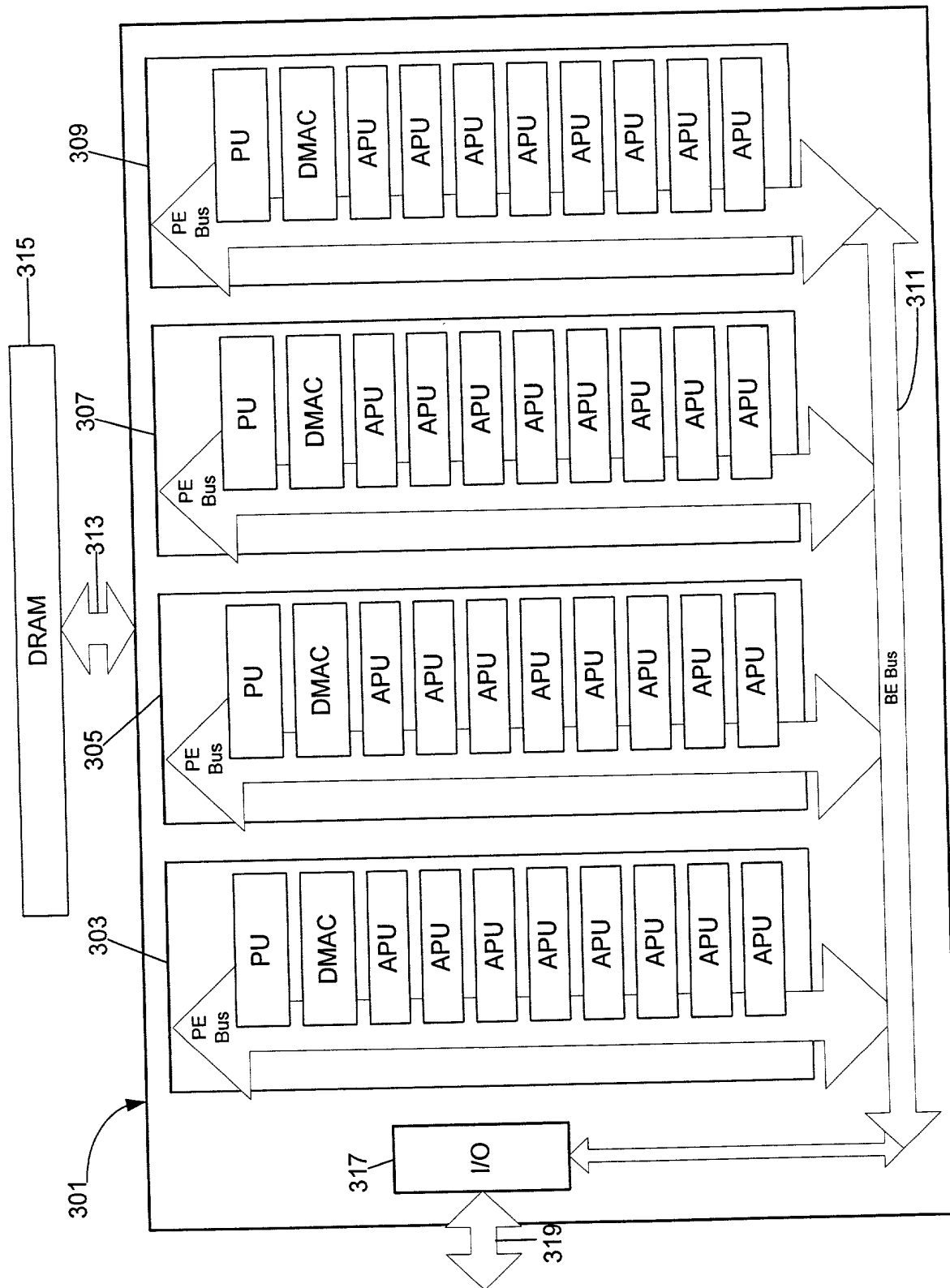


FIG. 3

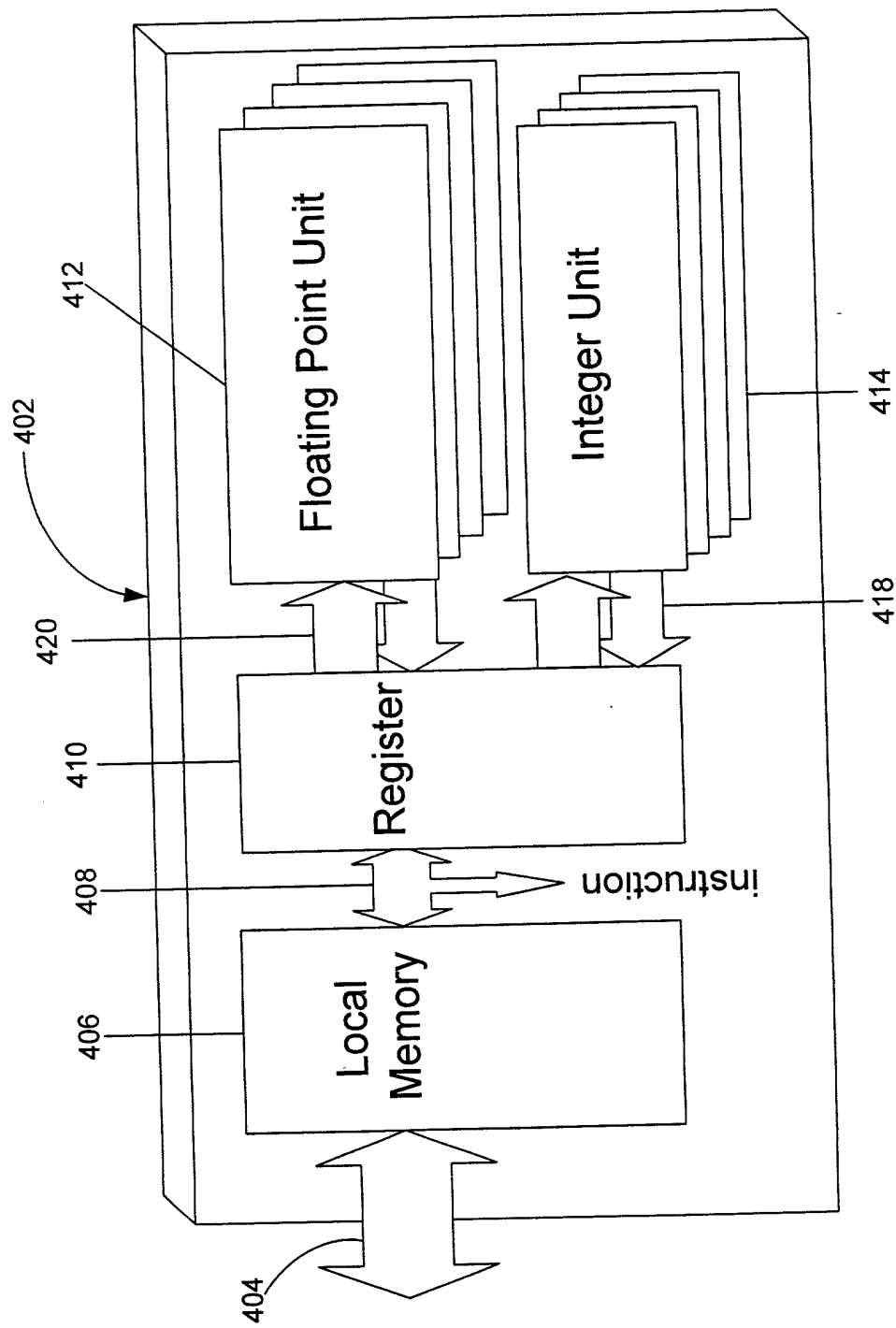


FIG. 4

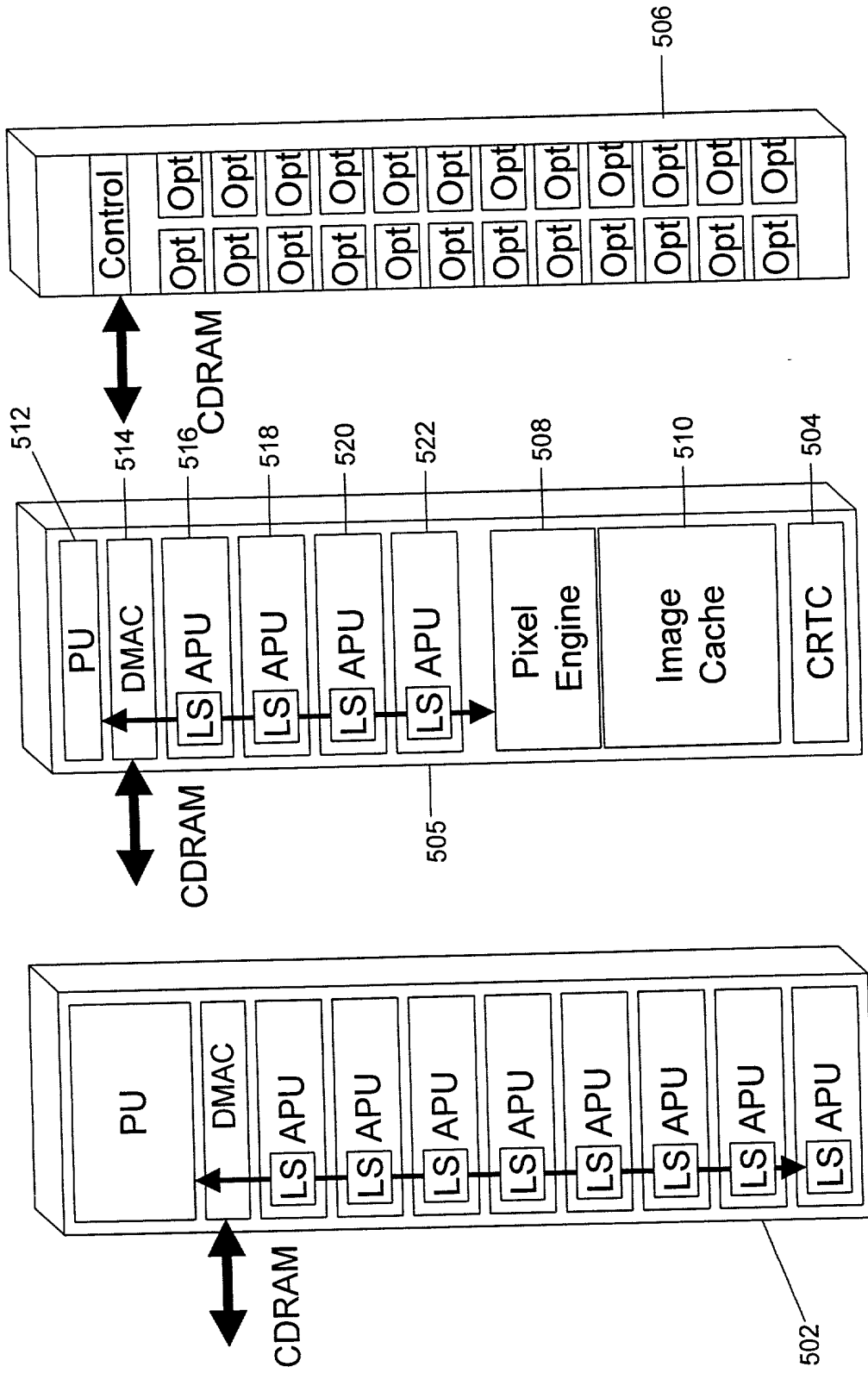


FIG. 5

US 2011/0270000 A1
Pub. No. 2011/0270000 A1
Pub. Date: Oct. 27, 2011
Pub. No. 2011/0270000 A1
Pub. Date: Oct. 27, 2011

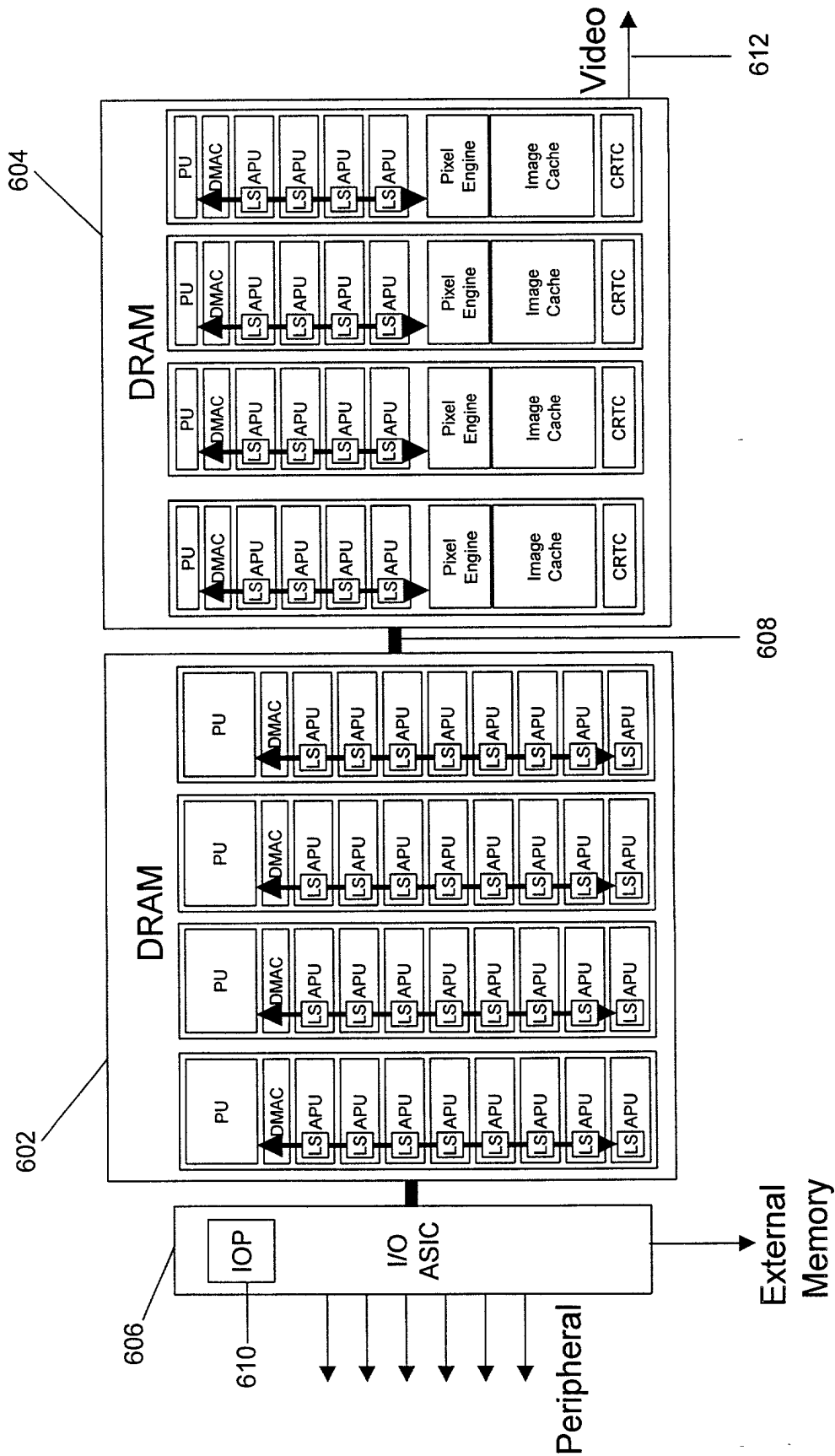


FIG. 6

Optical Fiber Link

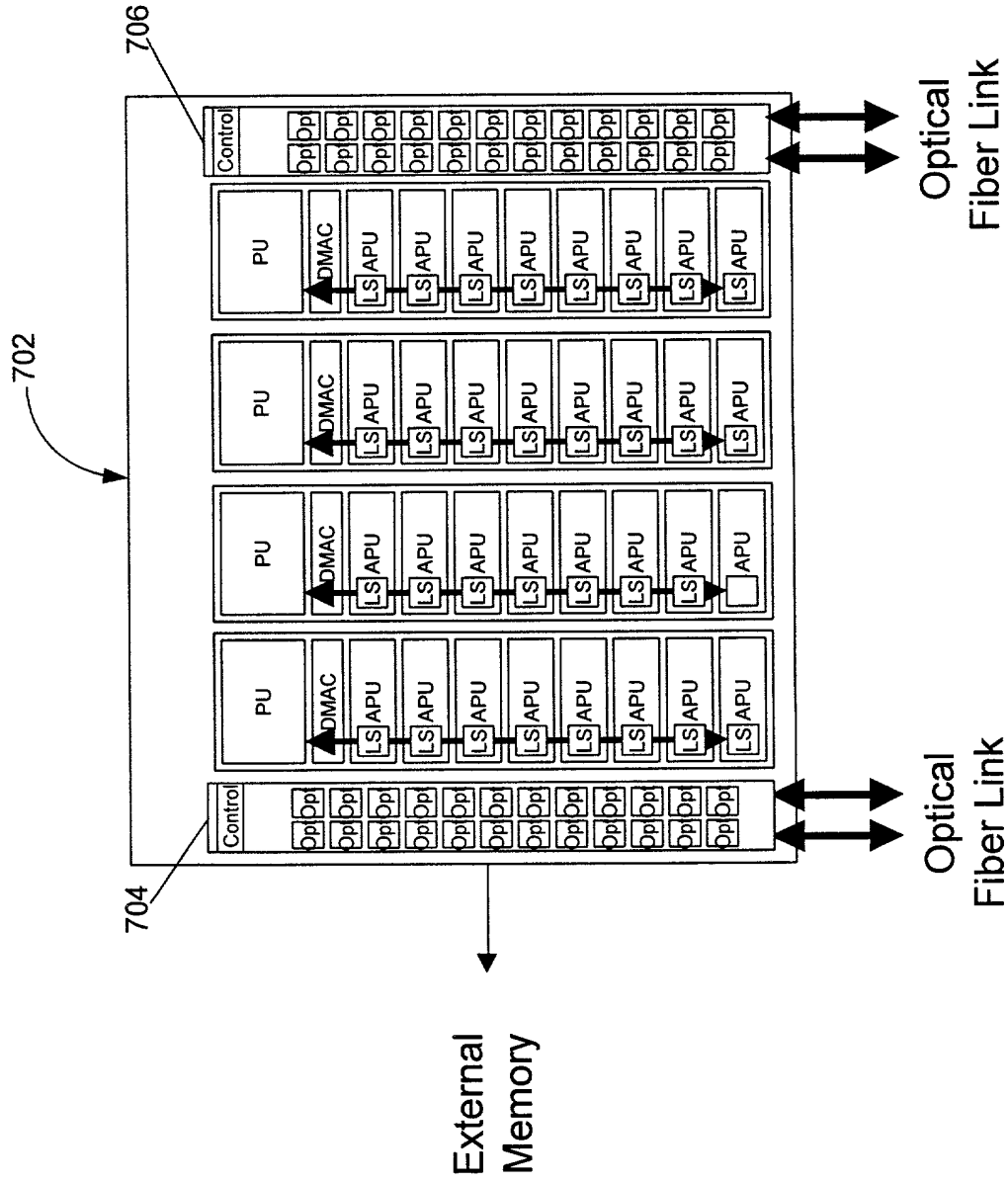


FIG. 7

1. A system comprising:
 a. a processor;
 b. a memory; and
 c. a video output device.

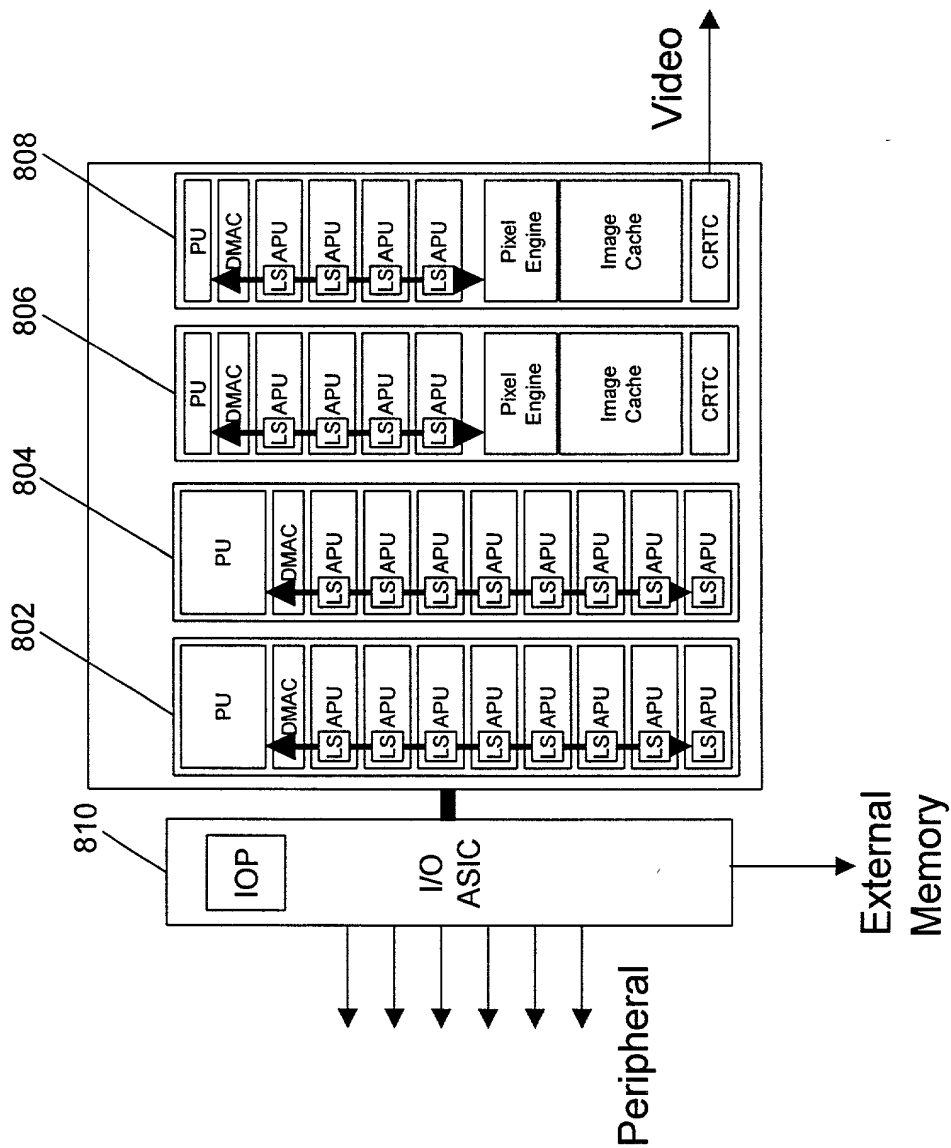


FIG. 8

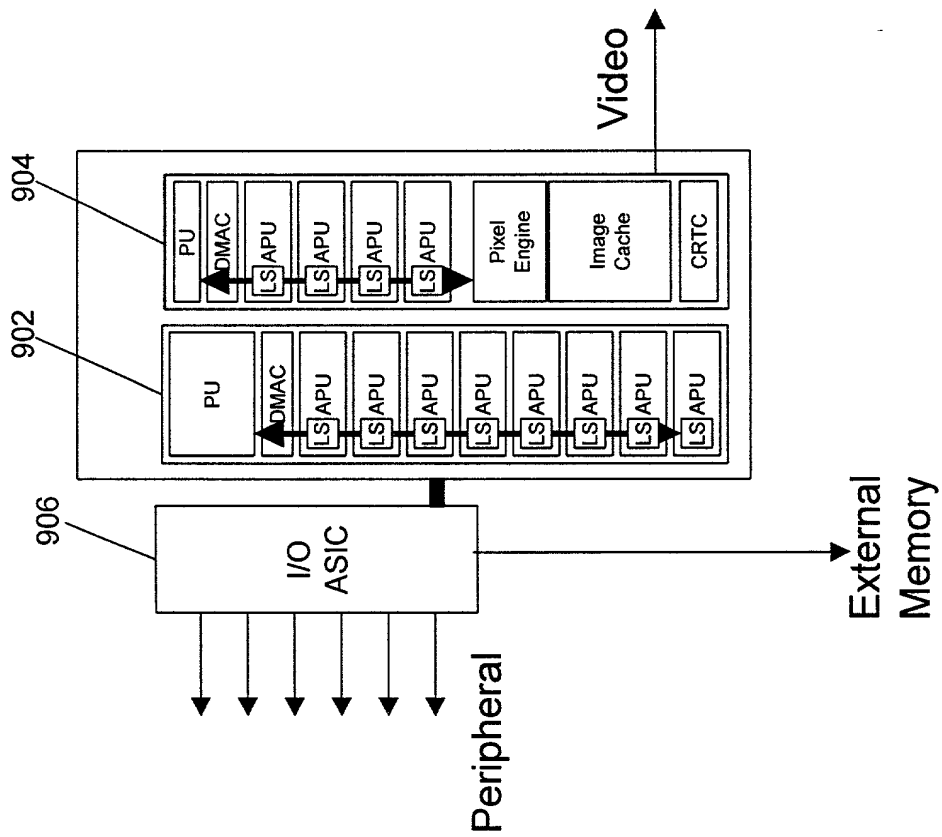


FIG. 9

FIG. 10 is a block diagram of a system architecture. The system includes a Peripheral (1004) connected to an I/O ASIC (1002). The I/O ASIC (1002) is connected to a PU (1002), which is connected to a DMAC. The DMAC is connected to a LSAPU, which is connected to a LSAPU, which is connected to a LSAPU, which is connected to a LSAPU. The LSAPU is connected to a Pixel Engine, which is connected to an Image Cache, which is connected to a CRT. The CRT is connected to a Video output.

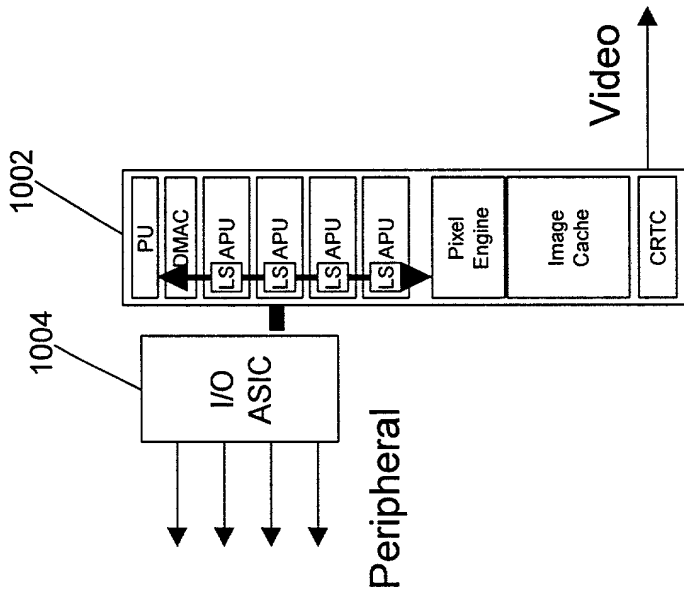


FIG. 10

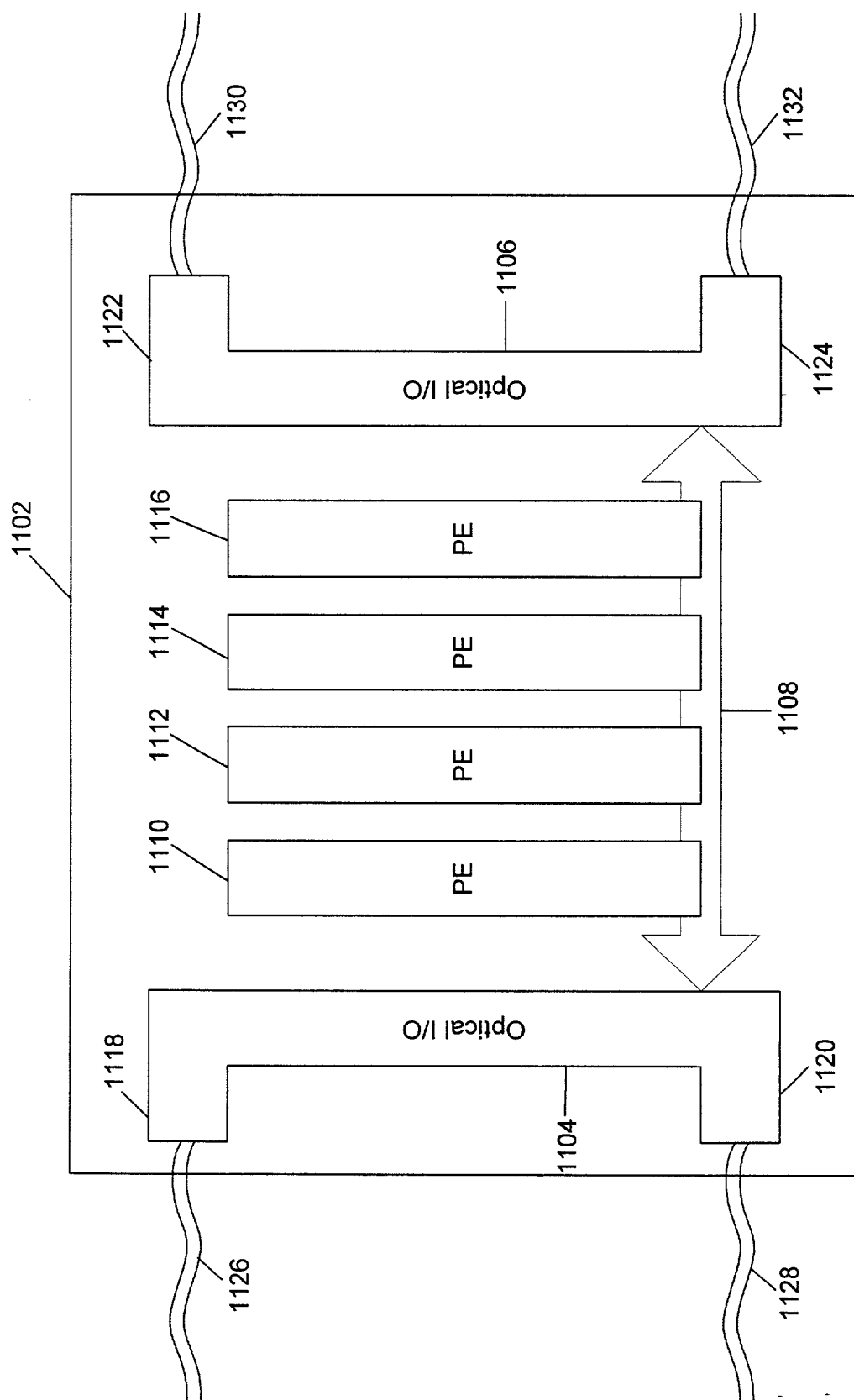


FIG. 11A

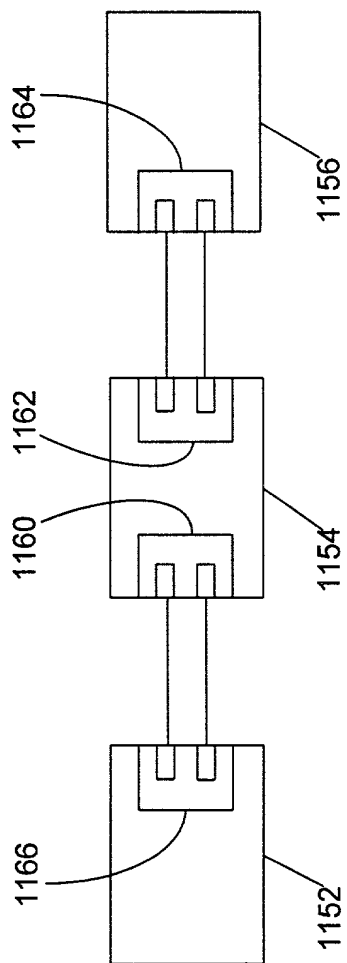


FIG. 11B

FIG. 11C is a schematic diagram of a system architecture. The system includes a first device 1172, a second device 1174, a third device 1176, a fourth device 1178, and a fifth device 1180. The first device 1172 is connected to the second device 1174, the third device 1176, and the fourth device 1178. The second device 1174 is connected to the third device 1176 and the fourth device 1178. The third device 1176 is connected to the fourth device 1178 and the fifth device 1180. The fourth device 1178 is connected to the fifth device 1180. The first device 1172 includes a first component 1188 and a second component 1190. The second device 1174 includes a third component 1182 and a fourth component 1184. The third device 1176 includes a fifth component 1186 and a sixth component 1188. The fourth device 1178 includes a seventh component 1190 and an eighth component 1192. The fifth device 1180 includes a ninth component 1194 and a tenth component 1196.

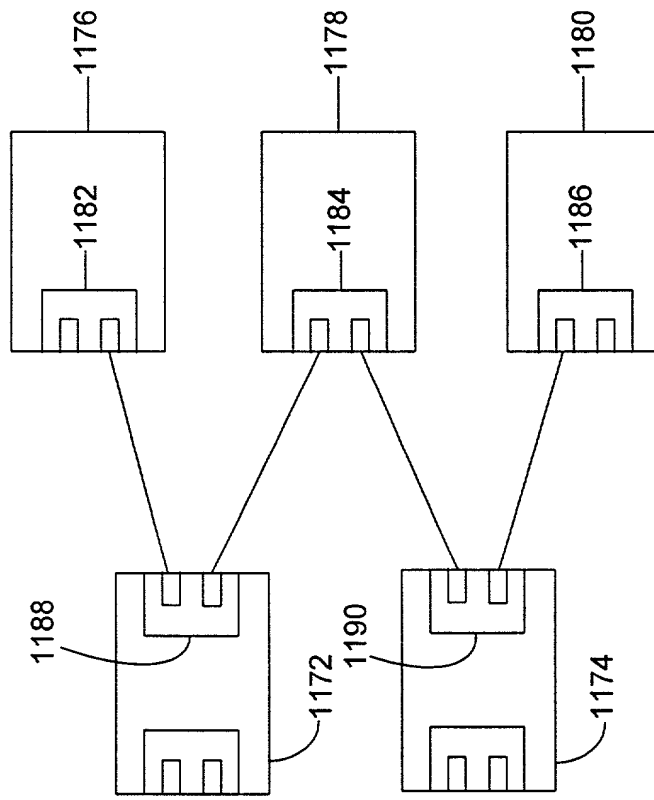


FIG. 11C

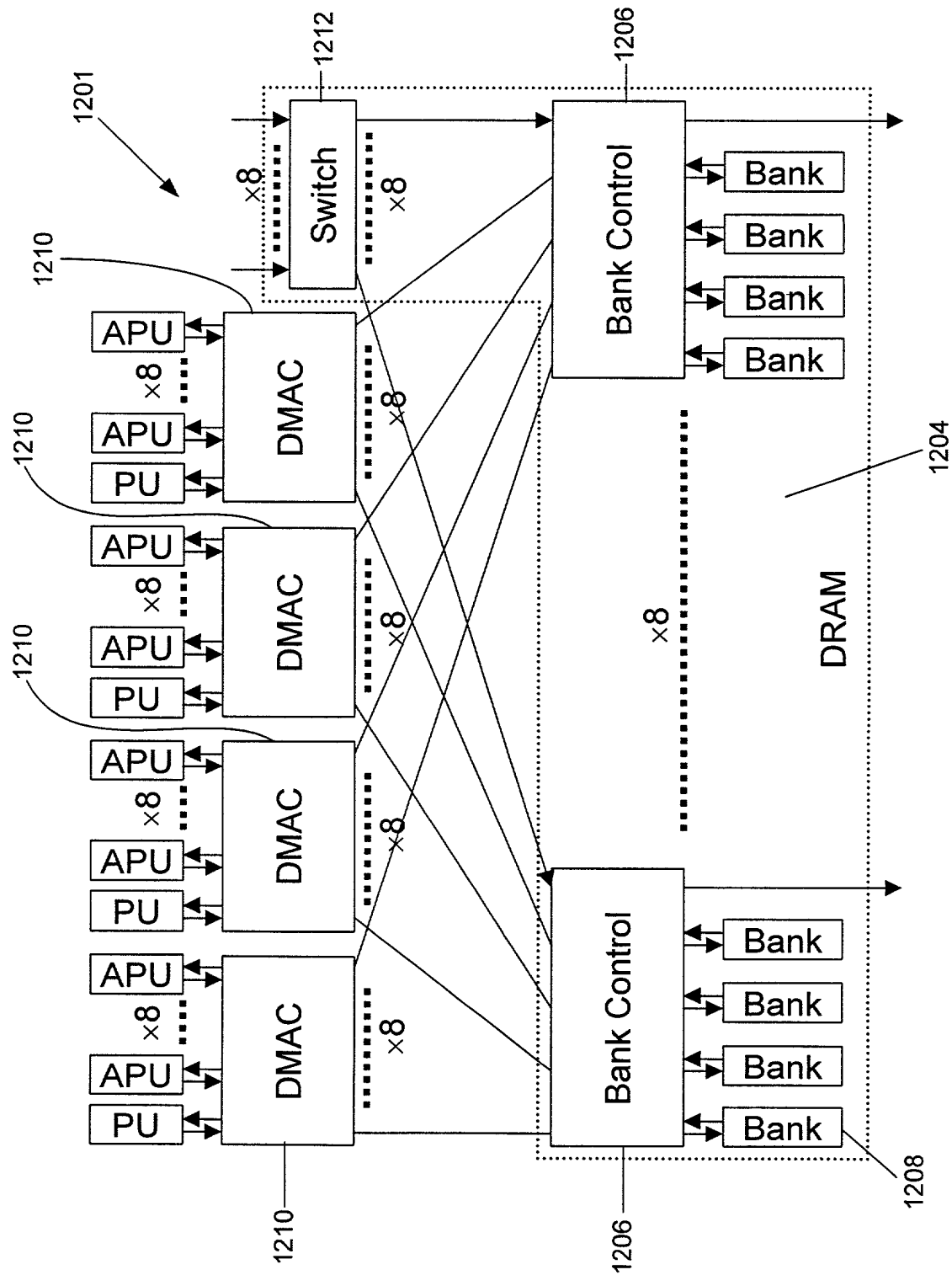


FIG. 12A

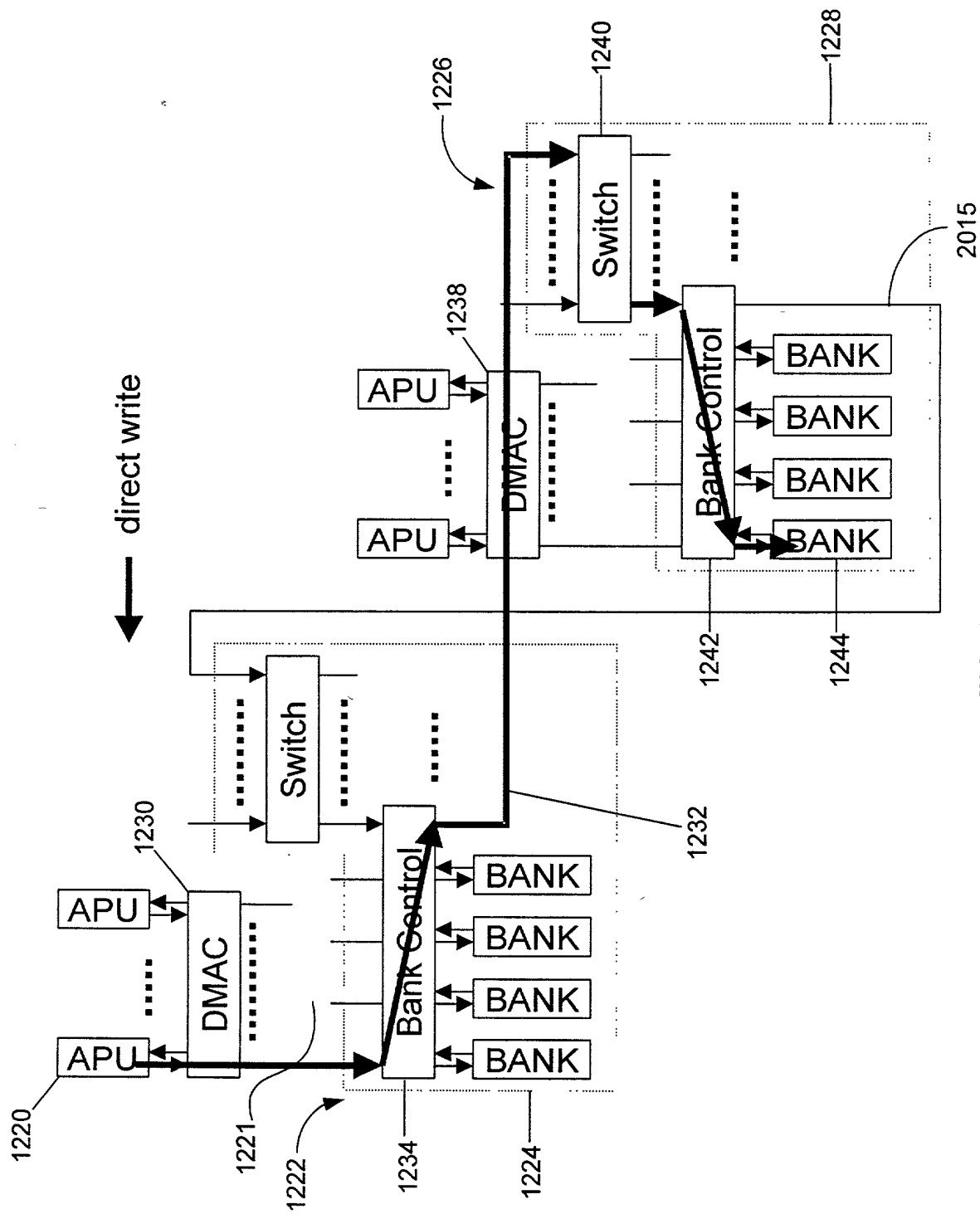
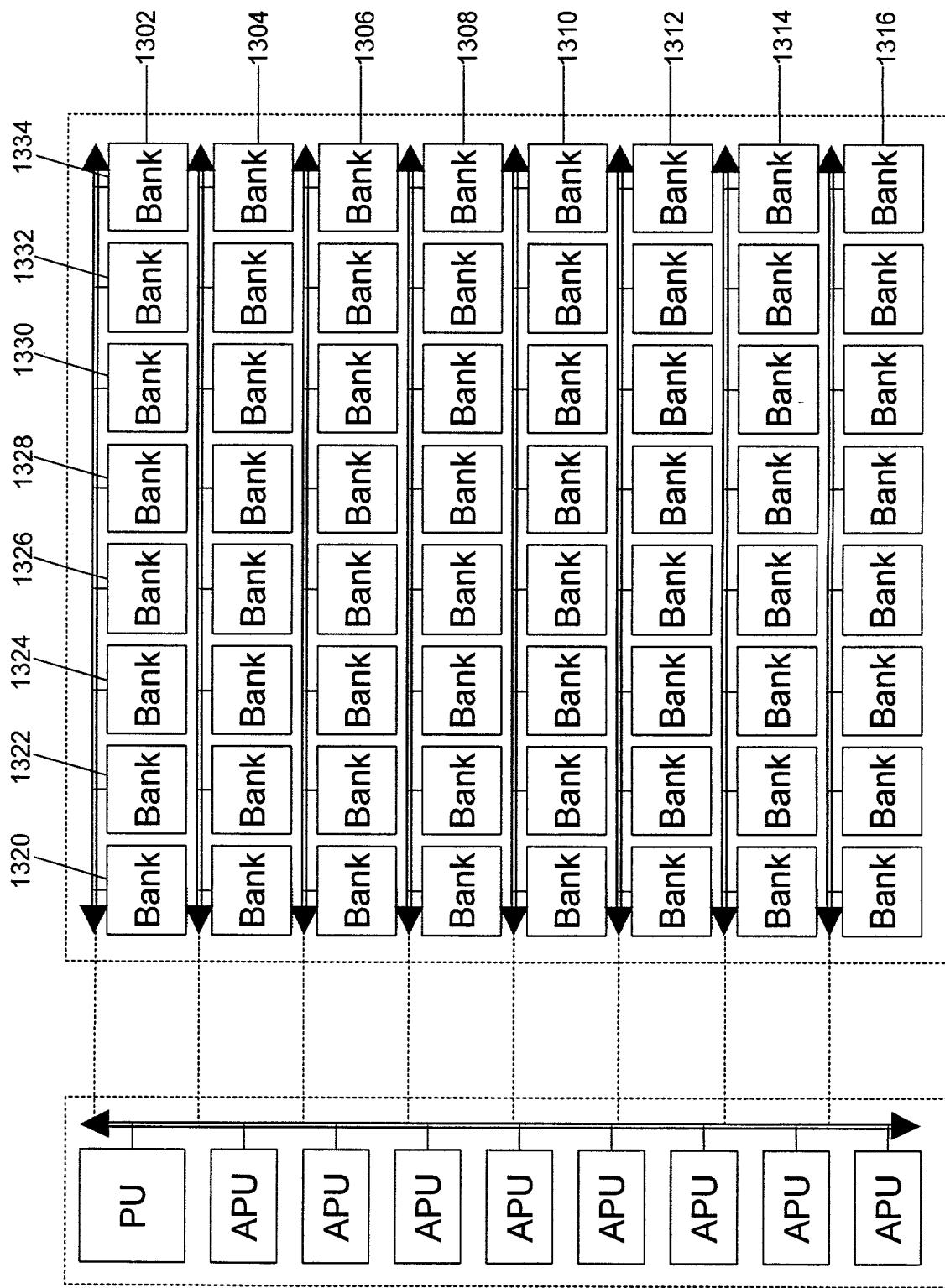


FIG. 12B

FIG. 13 is a block diagram of a system architecture. The system includes a PU (Processing Unit) and eight APUs (Application Processing Units). The PU is connected to the APUs via a bus. The APUs are connected to a DRAM (Dynamic Random Access Memory) via a bus. The DRAM is divided into eight banks, labeled 1302 through 1316. Each bank is connected to the APUs via a bus. The APUs are labeled 1320 through 1328. The banks are labeled 1330 through 1338. The bus is labeled 1340.



DRAM

FIG. 13

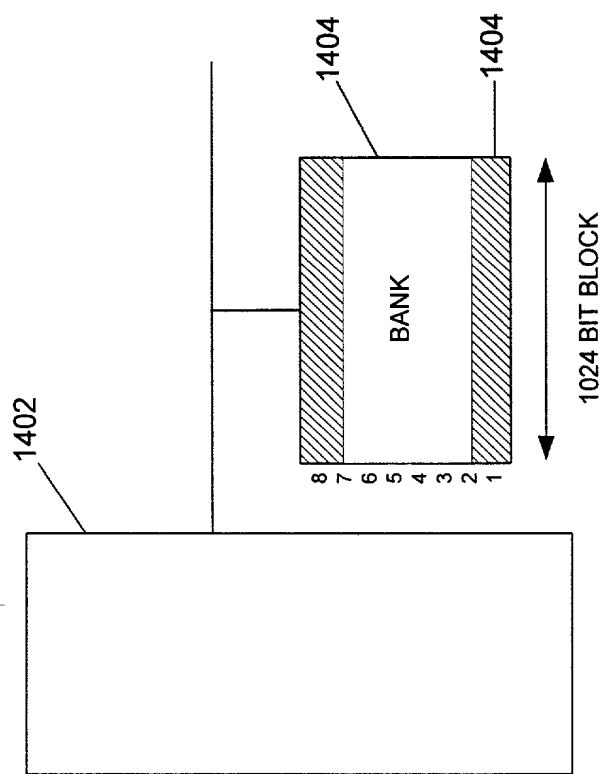


FIG. 14A

FIG. 14B is a block diagram of a memory system 1400. The memory system 1400 includes a memory controller 1412 and a memory array 1414. The memory array 1414 is divided into two banks, 1416 and 1418. Each bank is a 512-bit block.

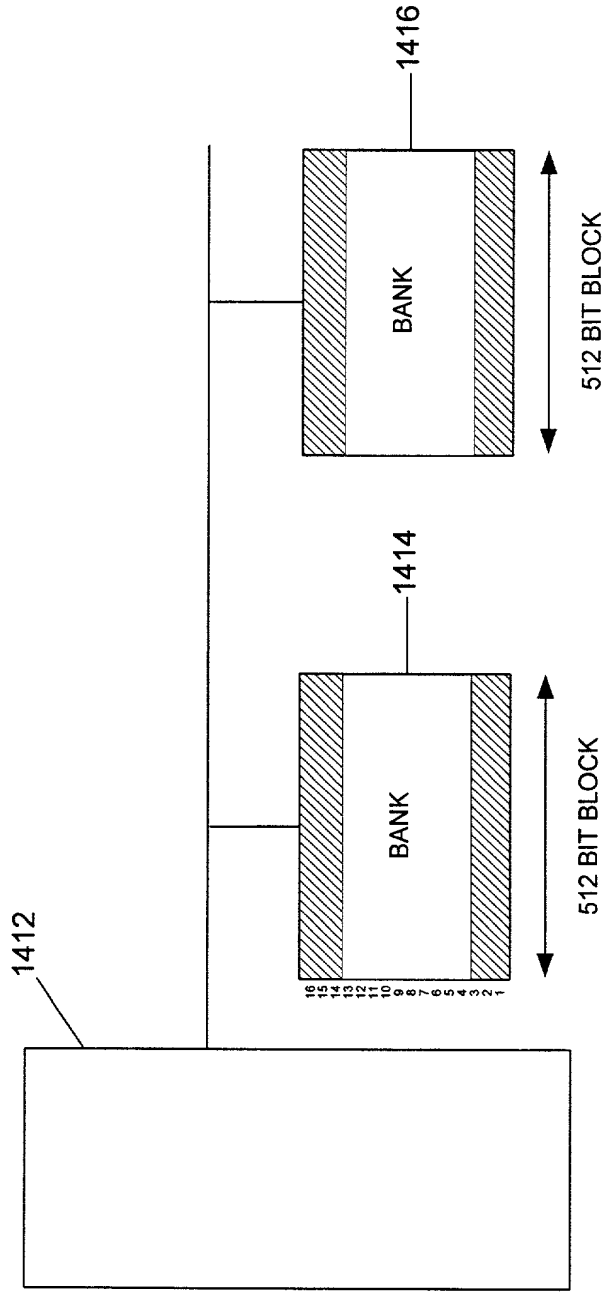


FIG. 14B

FIG. 15 is a block diagram of a system 1500. The system 1500 includes a processing unit (PU) 1502, a first application processing unit (APU) 1502, a second application processing unit (APU) 1502, and a third application processing unit (APU) 1502. The PU 1502 is connected to the first APU 1502. The first APU 1502 is connected to the second APU 1502. The second APU 1502 is connected to the third APU 1502. The first APU 1502 is also connected to a first switch 1504. The second APU 1502 is also connected to a second switch 1504. The third APU 1502 is also connected to a third switch 1504. The first switch 1504 is connected to a first output line 1506. The second switch 1504 is connected to a second output line 1506. The third switch 1504 is connected to a third output line 1506. The first output line 1506, the second output line 1506, and the third output line 1506 are connected to a common output line 1506.

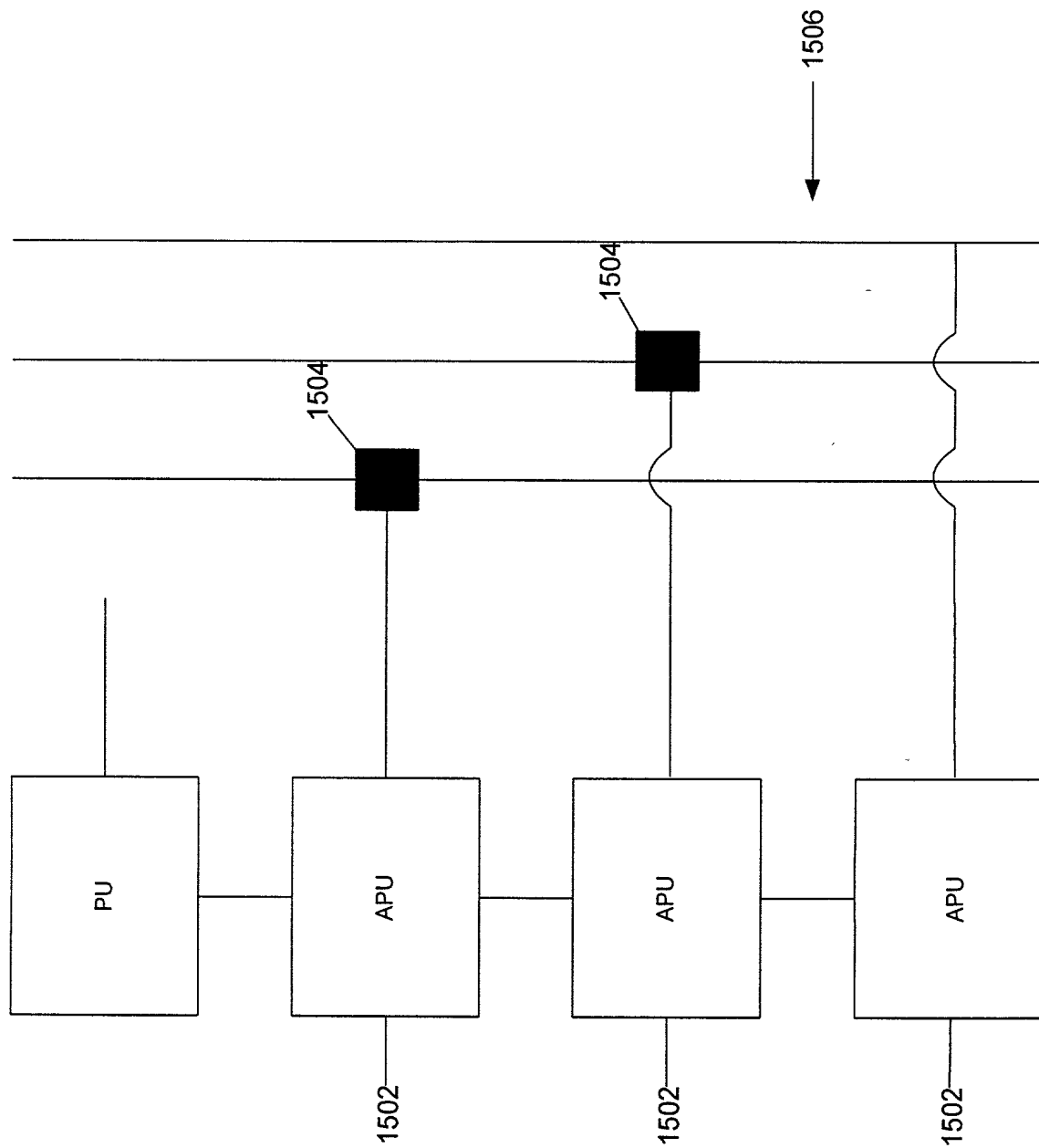


FIG. 15

FIG. 16 is a block diagram of a system 1600. The system 1600 includes a processing unit (PU) 1604, a data movement accelerator (DMA) 1606, and a set of application processors (APUs) 1602. The PU 1604, DMA 1606, and APUs 1602 are connected to a common bus 1607. The DMA 1606 is connected to a memory (DRAM) 1610 via a data path 1608. The APUs 1602 are connected to the bus 1607 via individual connections. The system 1600 is configured to perform data movement operations between the memory 1610 and the APUs 1602 using the DMA 1606.

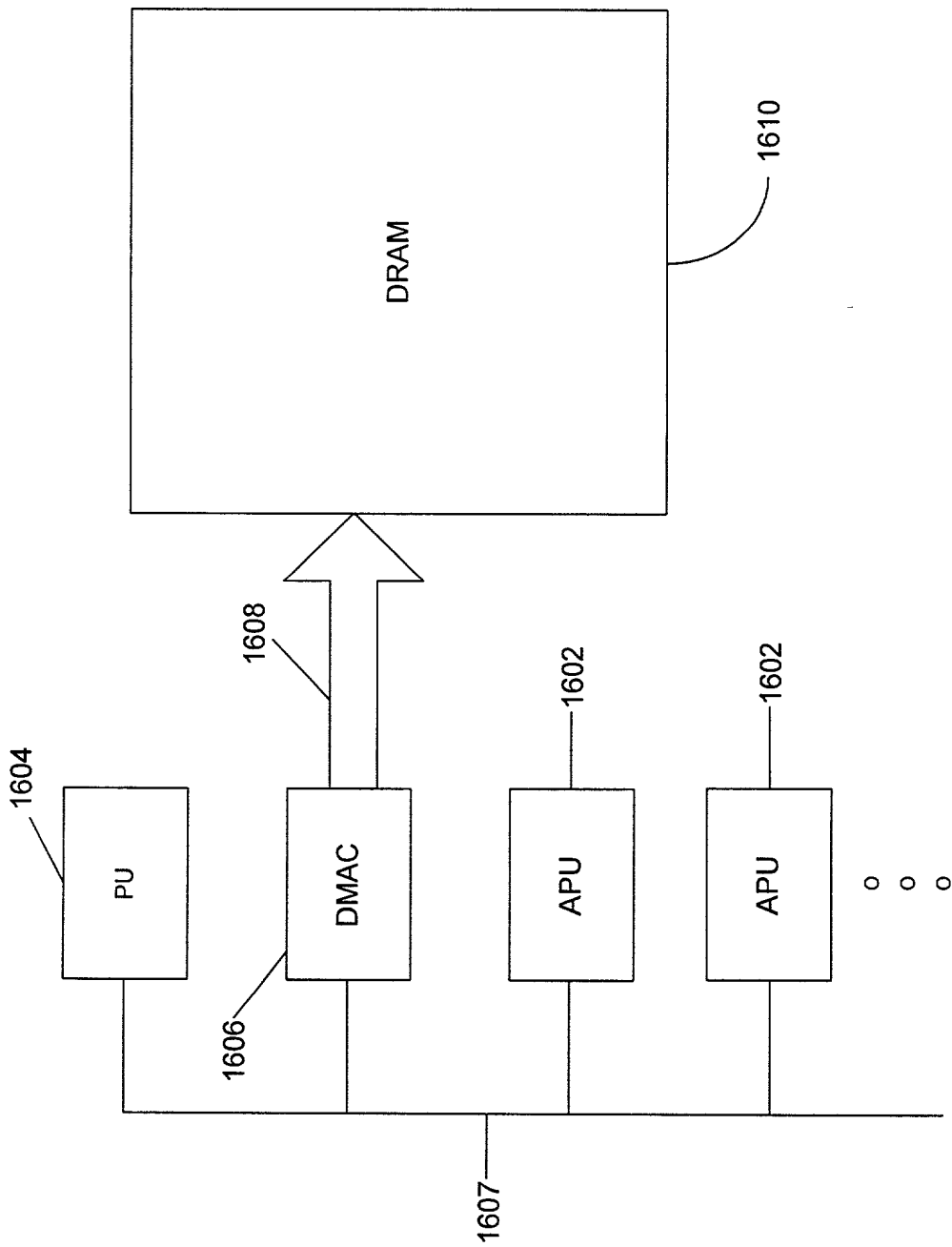


FIG. 16

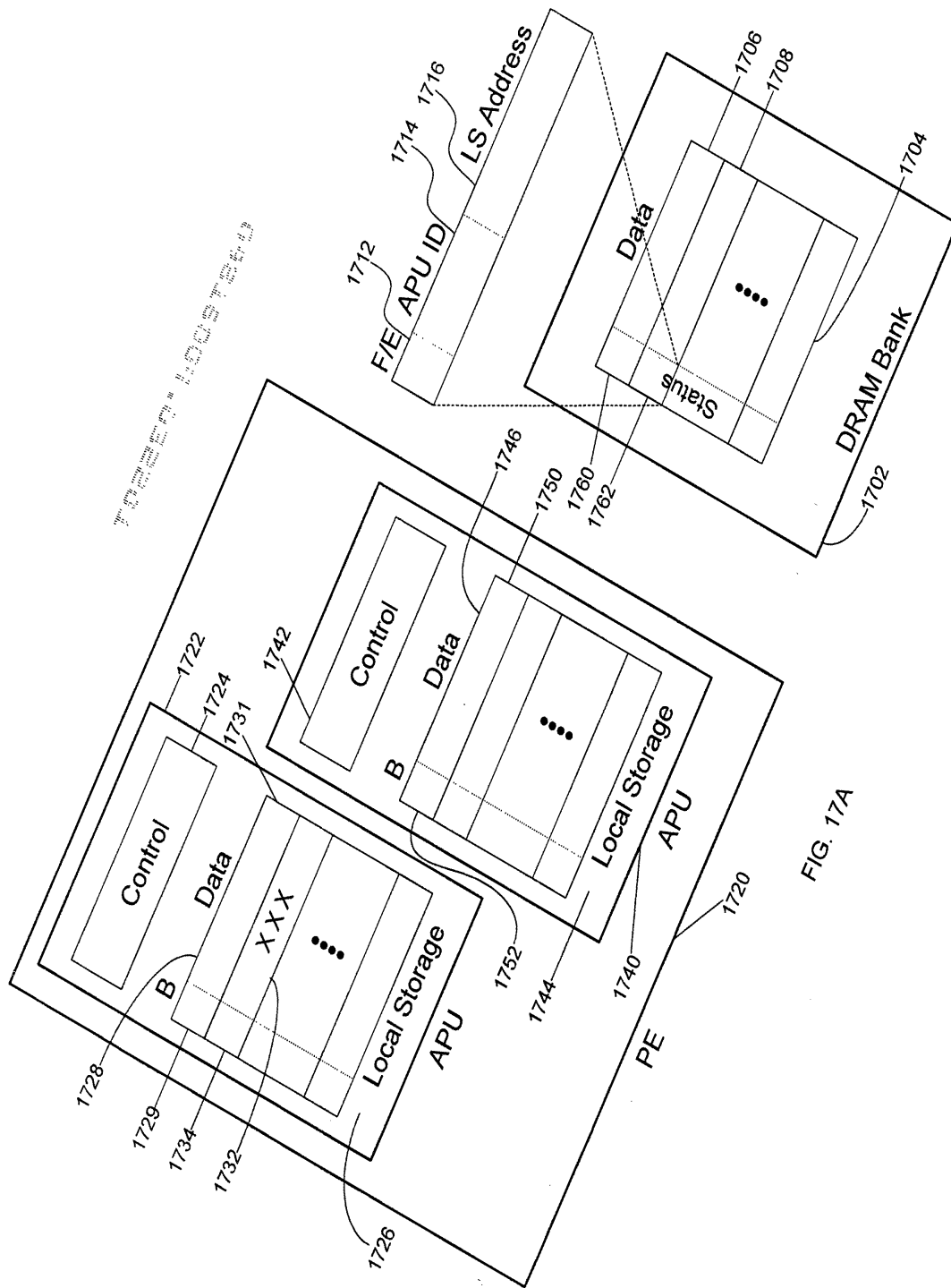


FIG. 17A

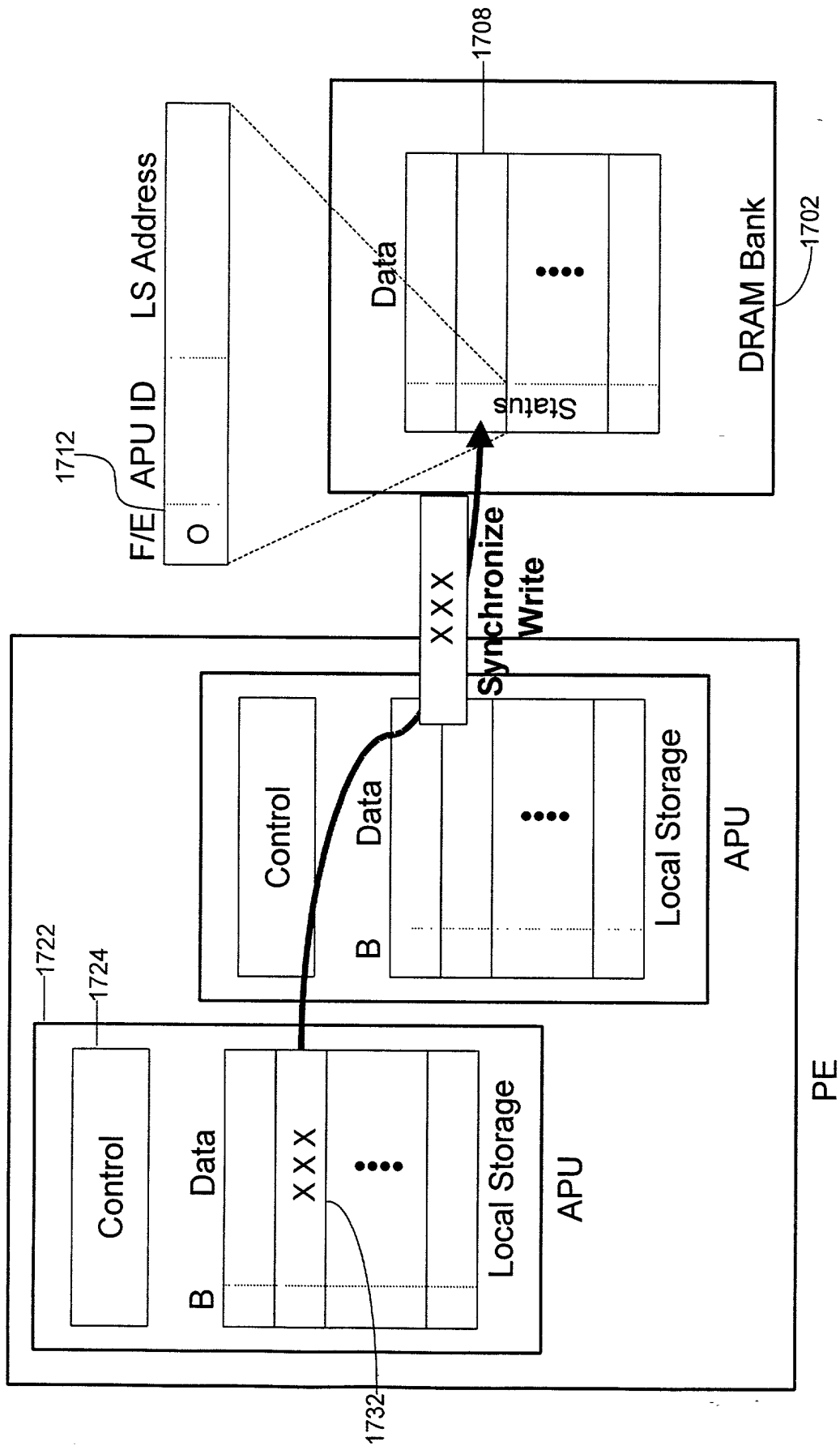


FIG. 17B

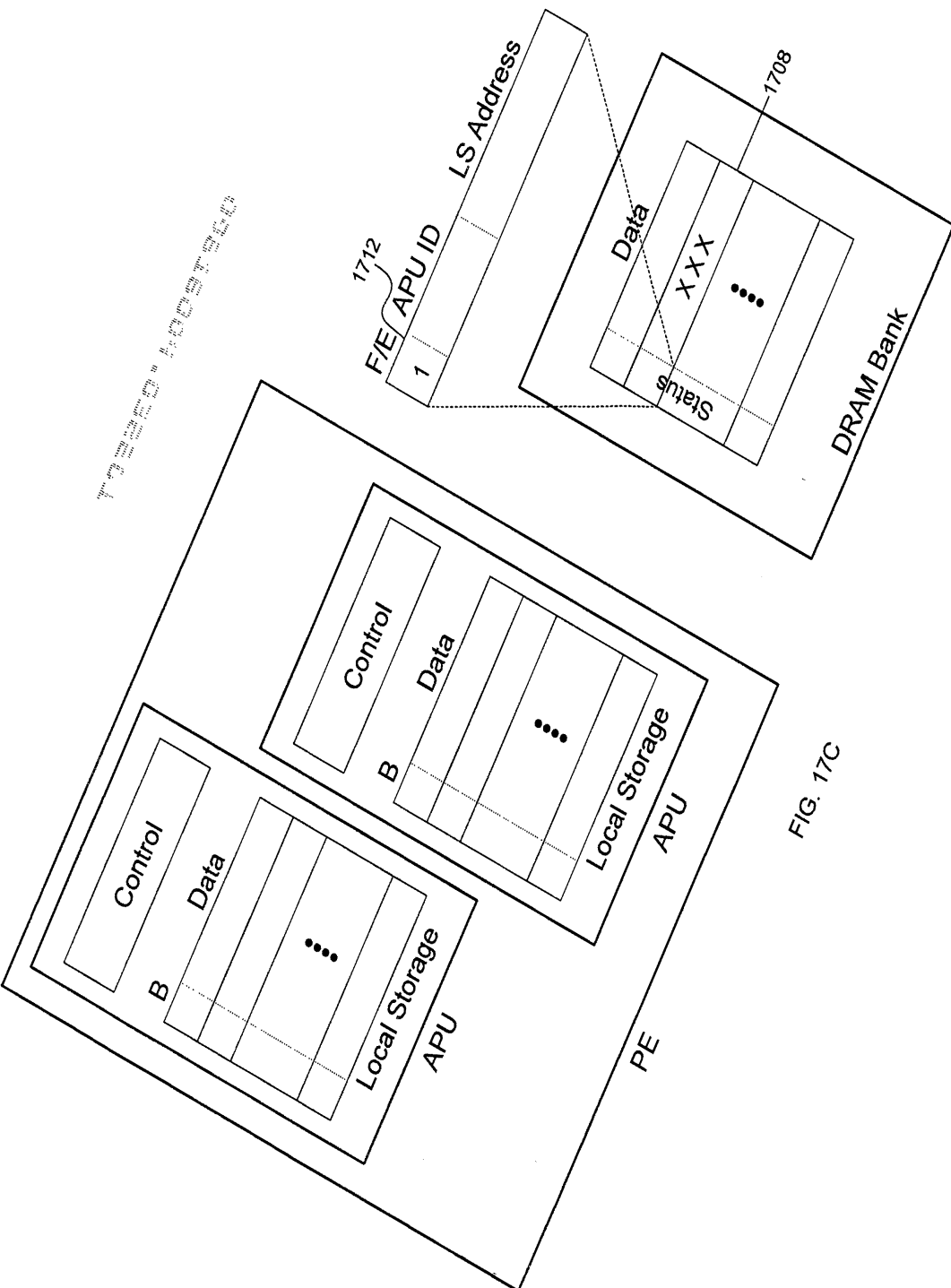


FIG. 17C

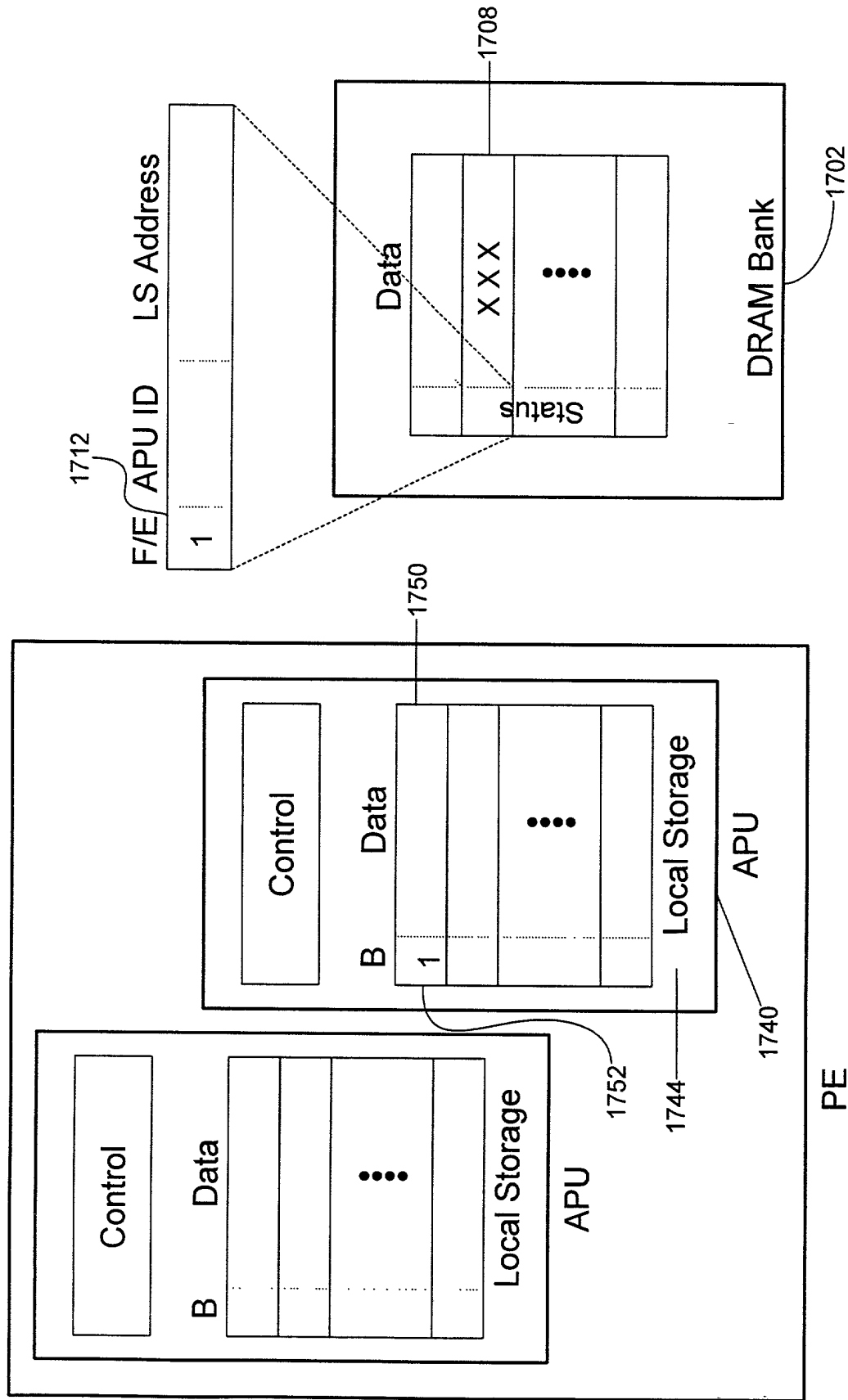


FIG. 17D

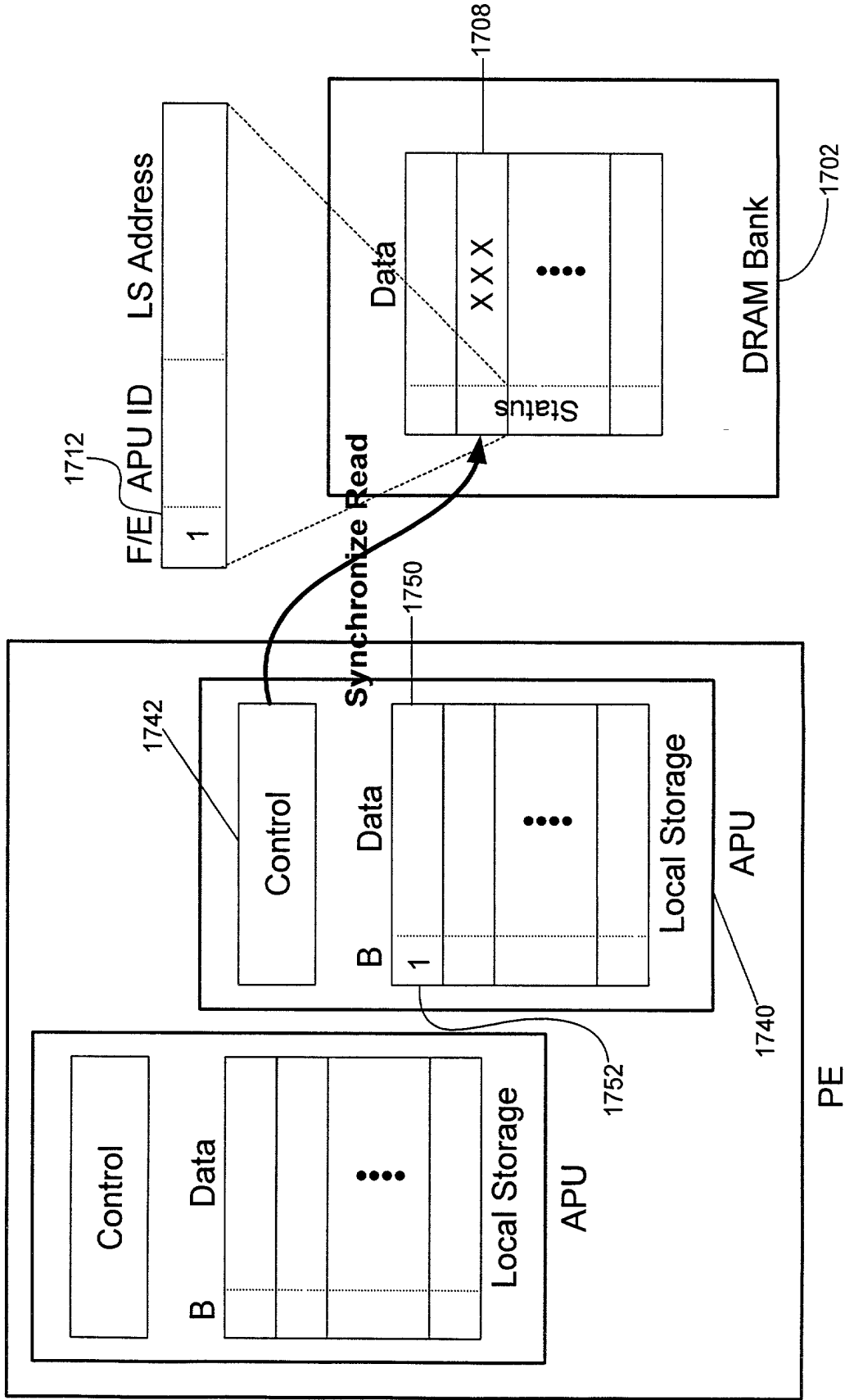


FIG. 17E

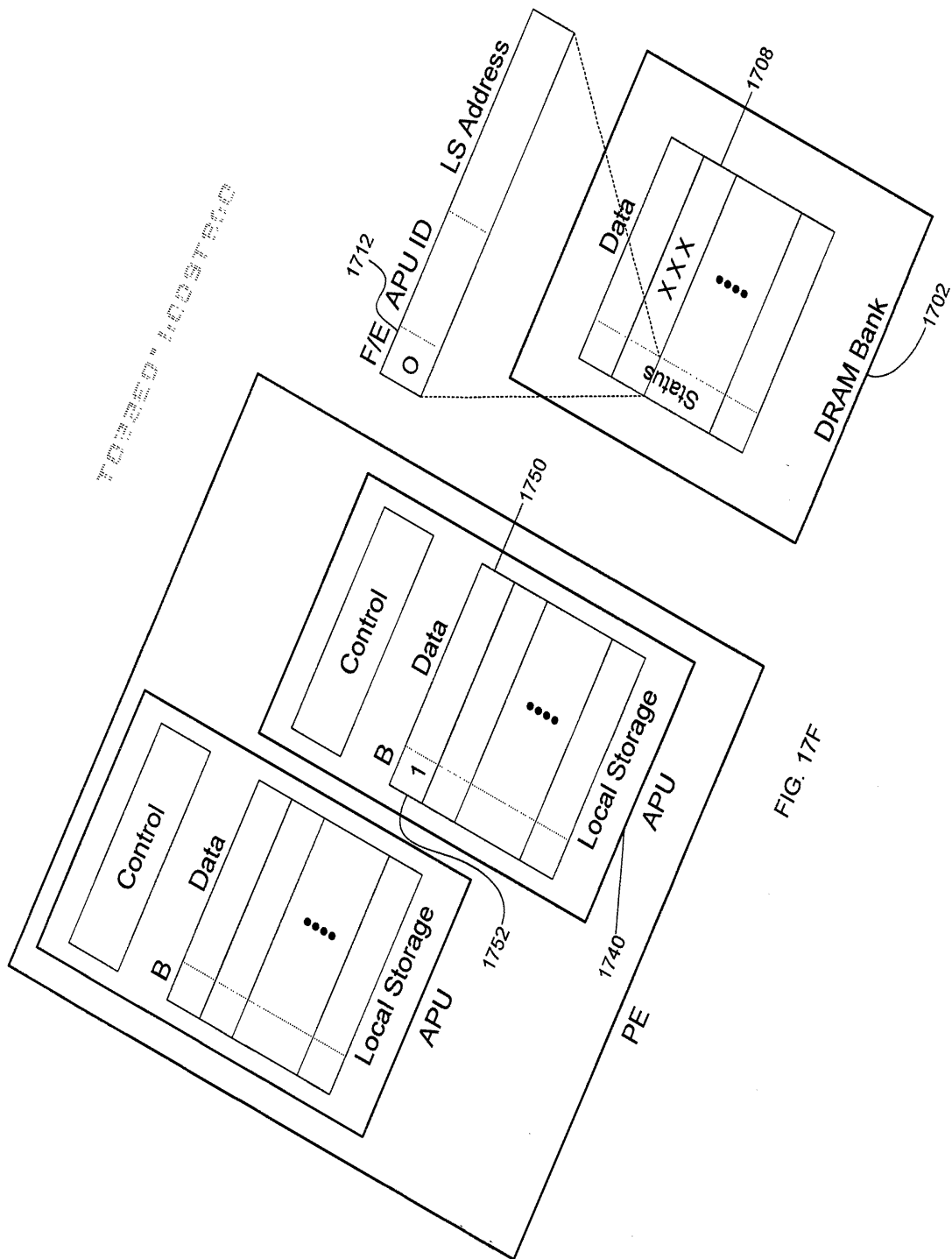


FIG. 17F

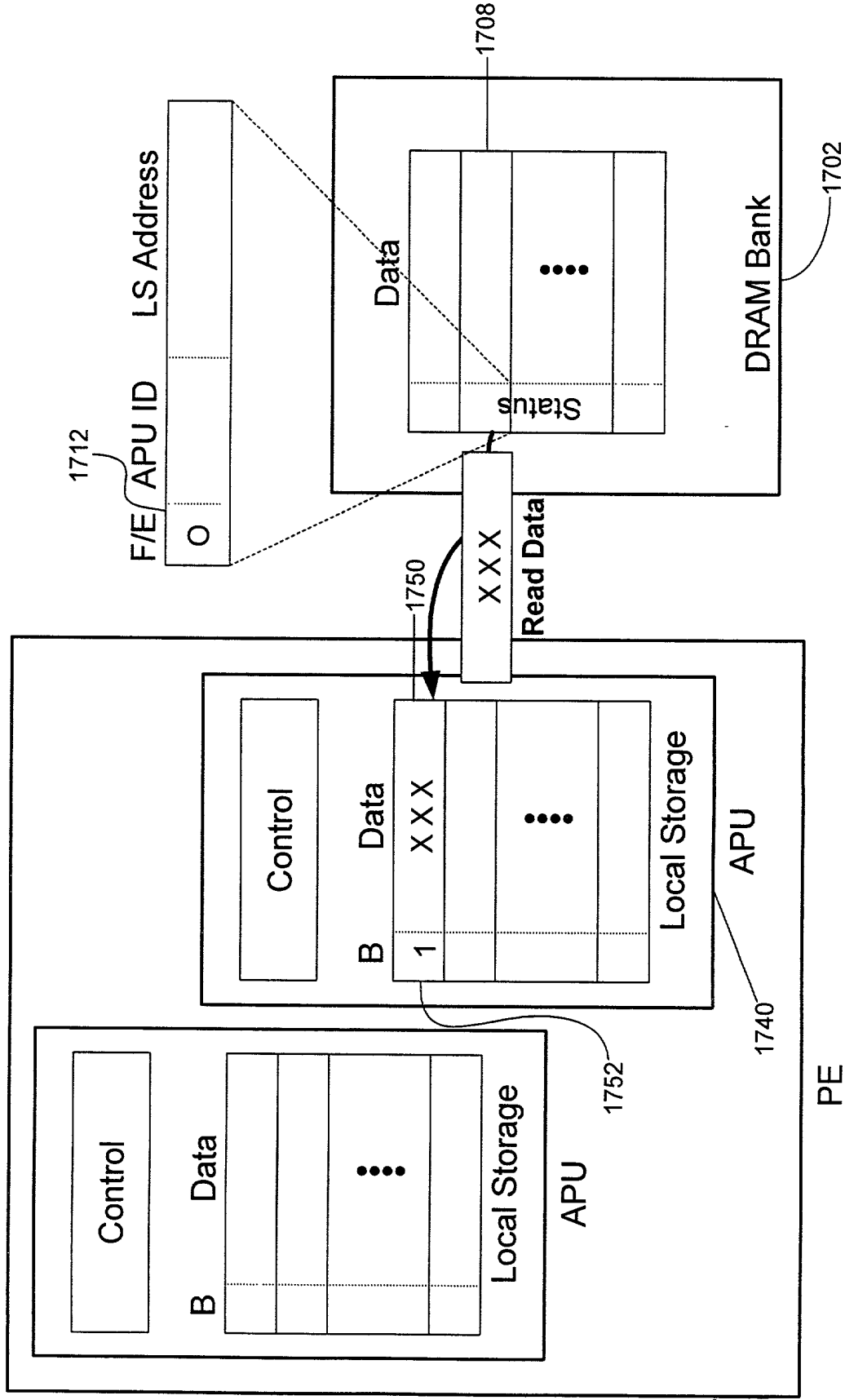


FIG. 17G

FIG. 17H

FIG. 17H

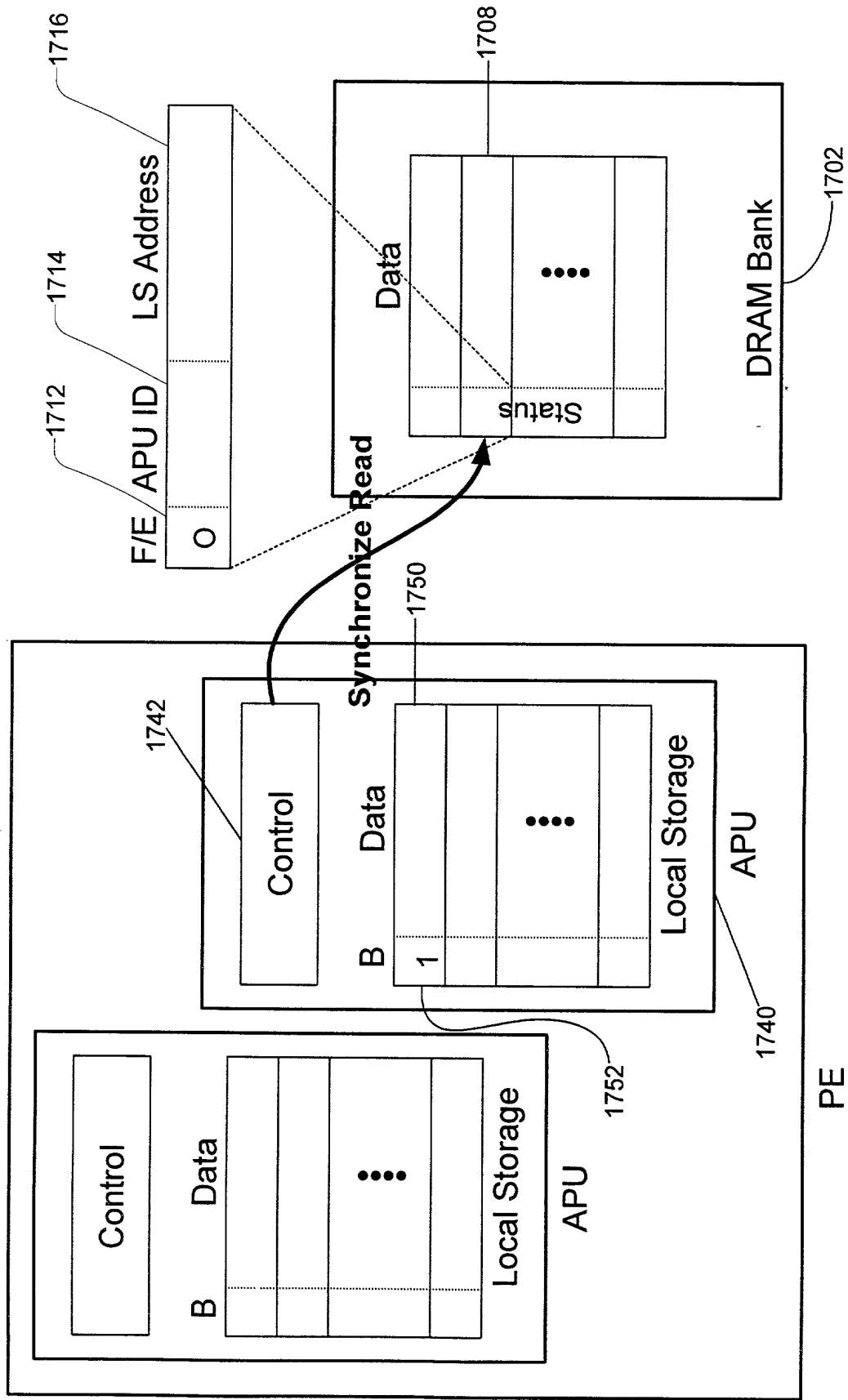


FIG. 17J

FIG. 17K is a block diagram of a processing element (PE) 1700, which is a component of a processing element array 1702. The PE 1700 includes a control unit 1742, a local storage unit 1744, and an APU 1740. The APU 1740 includes a control unit 1752, a local storage unit 1754, and a data unit 1750. The data unit 1750 is connected to a data bus 1708, which is connected to a data unit 1706. The data unit 1706 is connected to a data bus 1708, which is connected to a data unit 1706. The data unit 1706 is connected to a data bus 1708, which is connected to a data unit 1706.

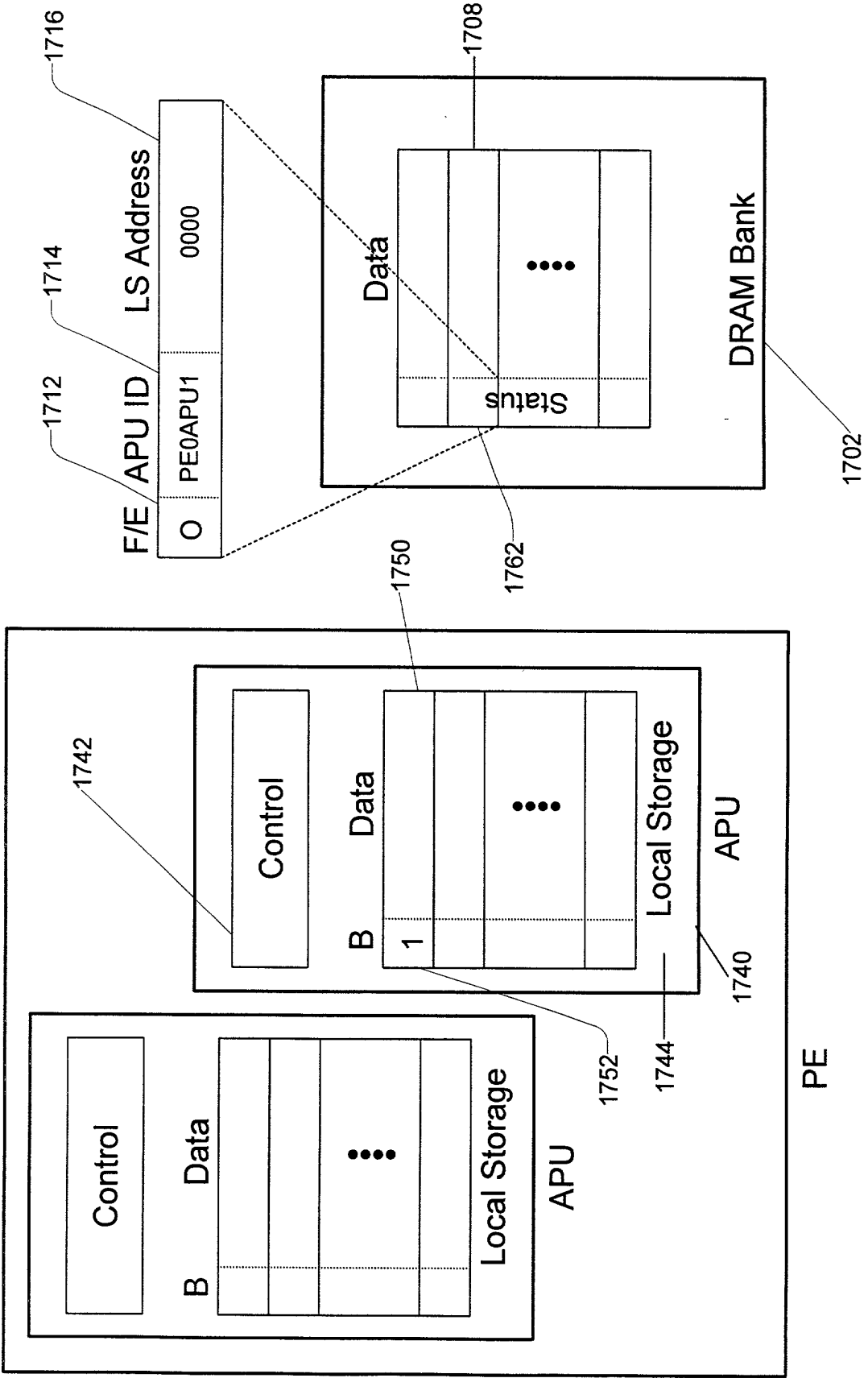


FIG. 17K

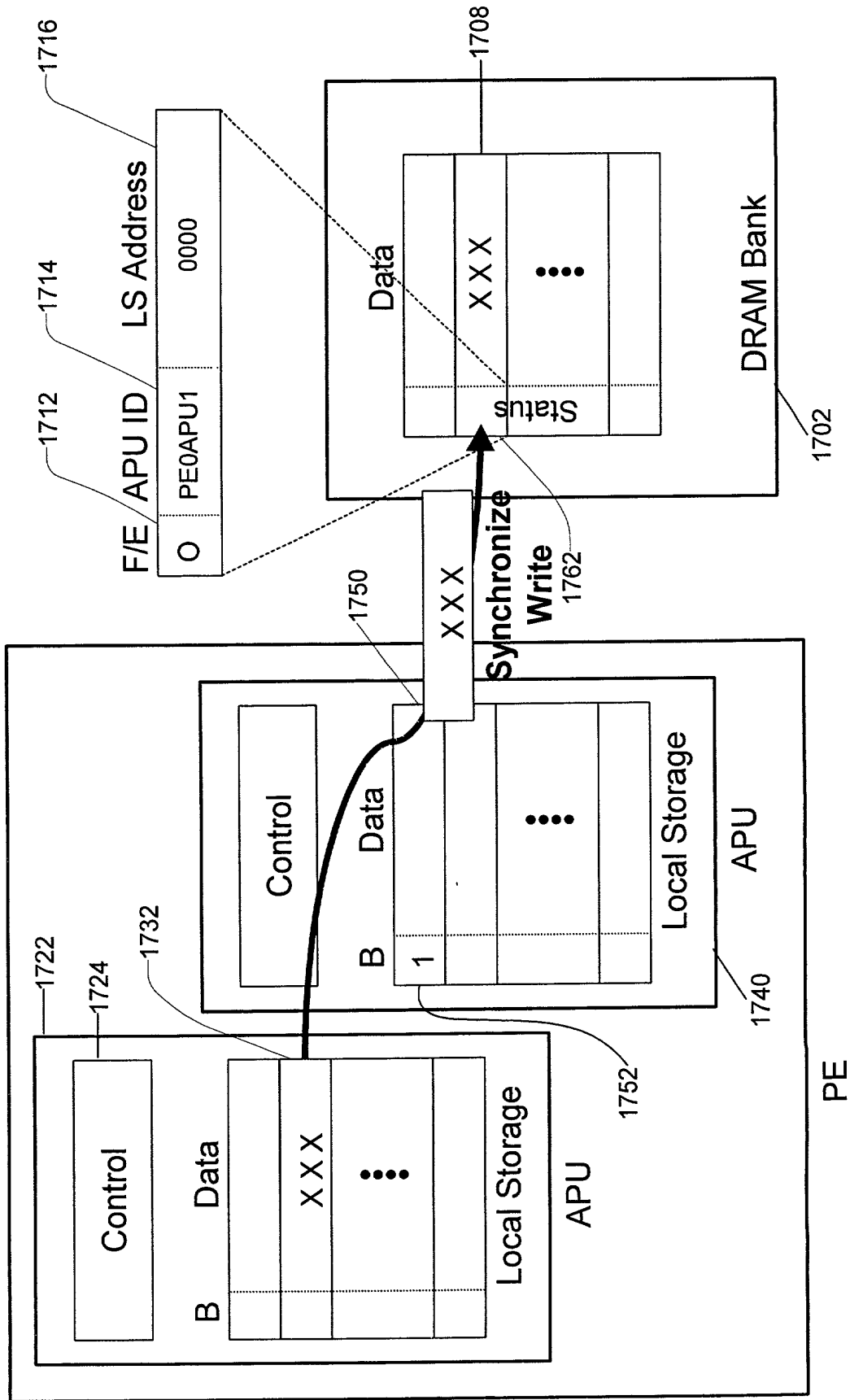


FIG. 17L

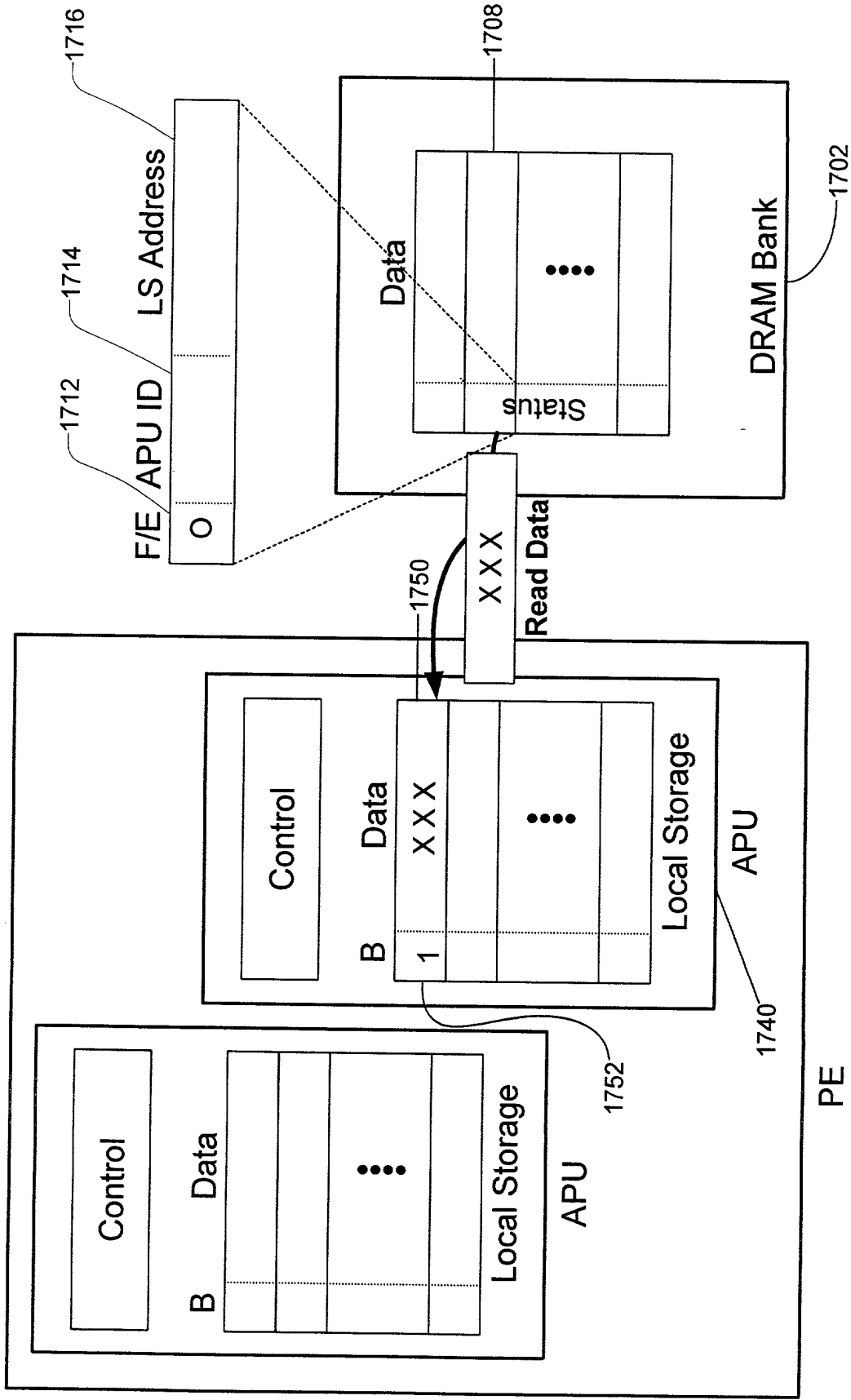
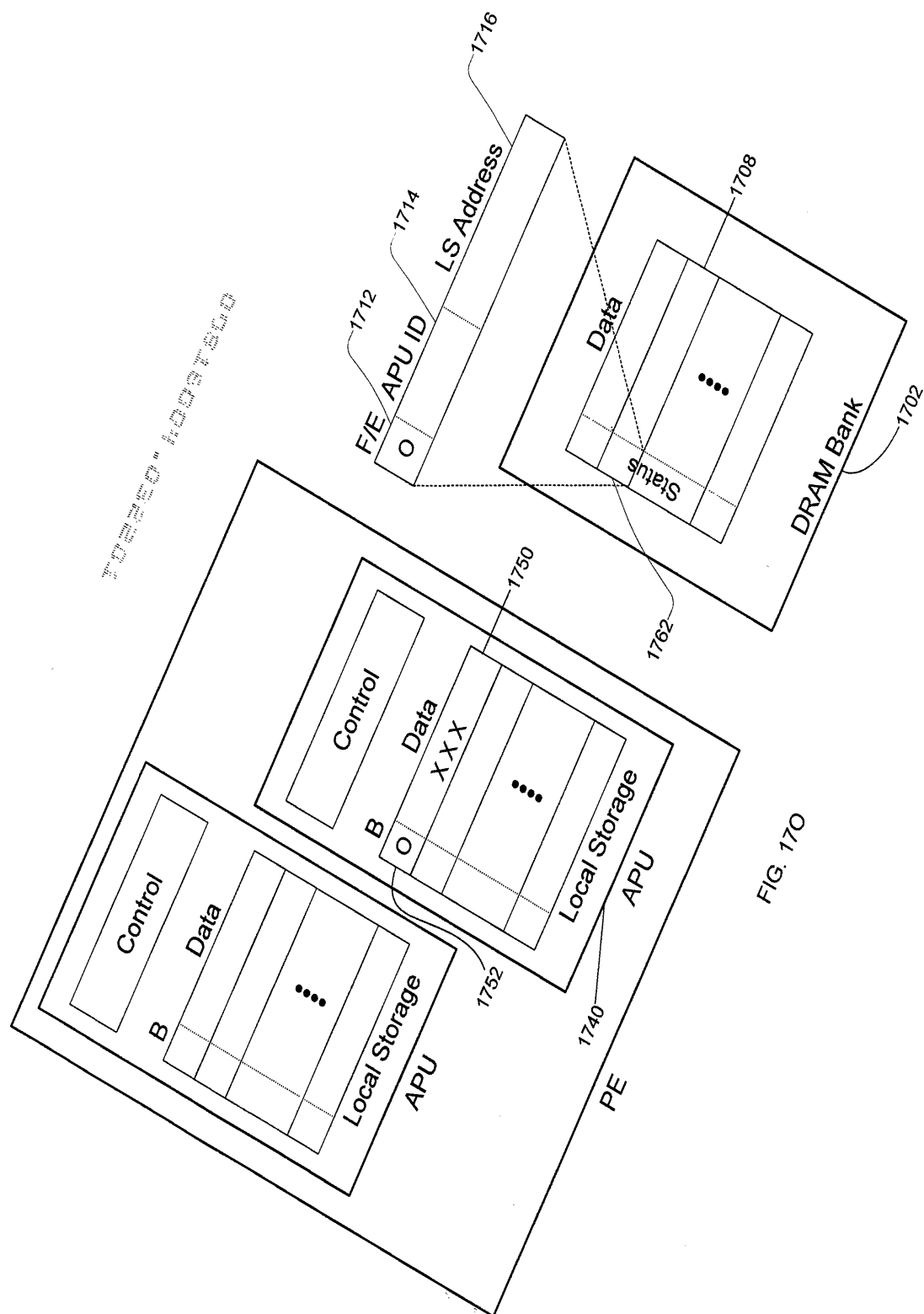


FIG. 17N



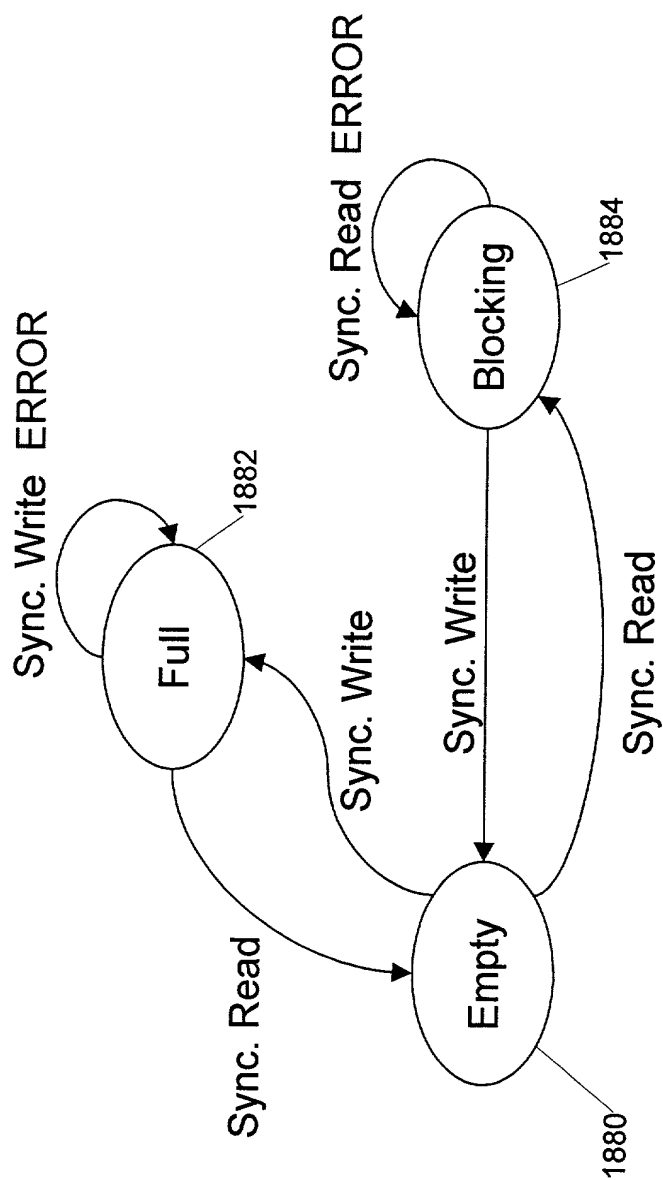


FIG. 18

FIG. 19 is a schematic diagram of a key control table 1902, which is a table that stores key information for each key ID. The table 1902 includes a key ID column 1904 and a key mask column 1906. The key ID column 1904 includes key IDs 0, 1, 2, ..., 7. The key mask column 1906 includes key masks for each key ID. The key mask for key ID 0 is "APU Key", the key mask for key ID 1 is "APU Key", the key mask for key ID 2 is "APU Key", and the key mask for key ID 7 is "APU Key".

Key Control Table

ID		1906	1908
0	APU Key	Key Mask	
1	APU Key	Key Mask	
2	APU Key	Key Mask	
		•	
		•	
		•	
		•	
		•	
		•	
7	APU Key	Key Mask	

FIG. 19

FIG. 20 is a schematic diagram of a data structure 2002, which may be a table or a database. The data structure 2002 includes a header 2006 and a body 2008. The header 2006 includes a key 2010 and a sync info 2012. The body 2008 includes a data column 2014 and a sync info column 2016. The data column 2014 includes a data row 2018 and a sync info row 2020. The sync info row 2020 includes a sync info cell 2022. The data row 2018 includes a data cell 2024. The data cell 2024 includes a data value 2026. The data value 2026 is a string of characters, such as "ABCDEF". The data value 2026 may be a binary value, such as "10101010". The data value 2026 may be a numerical value, such as "12345678". The data value 2026 may be a date, such as "2023-10-27". The data value 2026 may be a time, such as "10:10:10". The data value 2026 may be a location, such as "123 Main St, New York, NY 10001". The data value 2026 may be a person's name, such as "John Doe". The data value 2026 may be a company's name, such as "ABC Company". The data value 2026 may be a product's name, such as "XYZ Product". The data value 2026 may be a service's name, such as "DEF Service". The data value 2026 may be a category's name, such as "GHI Category". The data value 2026 may be a sub-category's name, such as "JKL Sub-category". The data value 2026 may be a specific item's name, such as "MNO Item". The data value 2026 may be a specific instance's name, such as "PQR Instance". The data value 2026 may be a specific event's name, such as "STU Event". The data value 2026 may be a specific action's name, such as "VWX Action". The data value 2026 may be a specific process's name, such as "YZA Process". The data value 2026 may be a specific task's name, such as "BCD Task". The data value 2026 may be a specific job's name, such as "EFG Job". The data value 2026 may be a specific project's name, such as "HIJ Project". The data value 2026 may be a specific program's name, such as "KLM Program". The data value 2026 may be a specific application's name, such as "NOP Application". The data value 2026 may be a specific system's name, such as "QRS System". The data value 2026 may be a specific network's name, such as "TUV Network". The data value 2026 may be a specific device's name, such as "WXY Device". The data value 2026 may be a specific component's name, such as "ZAB Component". The data value 2026 may be a specific part's name, such as "CDE Part". The data value 2026 may be a specific material's name, such as "FGH Material". The data value 2026 may be a specific resource's name, such as "IJK Resource". The data value 2026 may be a specific asset's name, such as "LMN Asset". The data value 2026 may be a specific liability's name, such as "OPQ Liability". The data value 2026 may be a specific obligation's name, such as "RST Obligation". The data value 2026 may be a specific responsibility's name, such as "UVW Responsibility". The data value 2026 may be a specific role's name, such as "XYZ Role". The data value 2026 may be a specific position's name, such as "ABC Position". The data value 2026 may be a specific title's name, such as "DEF Title". The data value 2026 may be a specific rank's name, such as "GHI Rank". The data value 2026 may be a specific grade's name, such as "JKL Grade". The data value 2026 may be a specific level's name, such as "MNO Level". The data value 2026 may be a specific stage's name, such as "PQR Stage". The data value 2026 may be a specific phase's name, such as "STU Phase". The data value 2026 may be a specific step's name, such as "VWX Step". The data value 2026 may be a specific process's name, such as "YZA Process". The data value 2026 may be a specific task's name, such as "BCD Task". The data value 2026 may be a specific job's name, such as "EFG Job". The data value 2026 may be a specific project's name, such as "HIJ Project". The data value 2026 may be a specific program's name, such as "KLM Program". The data value 2026 may be a specific application's name, such as "NOP Application". The data value 2026 may be a specific system's name, such as "QRS System". The data value 2026 may be a specific network's name, such as "TUV Network". The data value 2026 may be a specific device's name, such as "WXY Device". The data value 2026 may be a specific component's name, such as "ZAB Component". The data value 2026 may be a specific part's name, such as "CDE Part". The data value 2026 may be a specific material's name, such as "FGH Material". The data value 2026 may be a specific resource's name, such as "IJK Resource". The data value 2026 may be a specific asset's name, such as "LMN Asset". The data value 2026 may be a specific liability's name, such as "OPQ Liability". The data value 2026 may be a specific obligation's name, such as "RST Obligation". The data value 2026 may be a specific responsibility's name, such as "UVW Responsibility". The data value 2026 may be a specific role's name, such as "XYZ Role". The data value 2026 may be a specific position's name, such as "ABC Position". The data value 2026 may be a specific title's name, such as "DEF Title". The data value 2026 may be a specific rank's name, such as "GHI Rank". The data value 2026 may be a specific grade's name, such as "JKL Grade". The data value 2026 may be a specific level's name, such as "MNO Level". The data value 2026 may be a specific stage's name, such as "PQR Stage". The data value 2026 may be a specific phase's name, such as "STU Phase". The data value 2026 may be a specific step's name, such as "VWX Step".

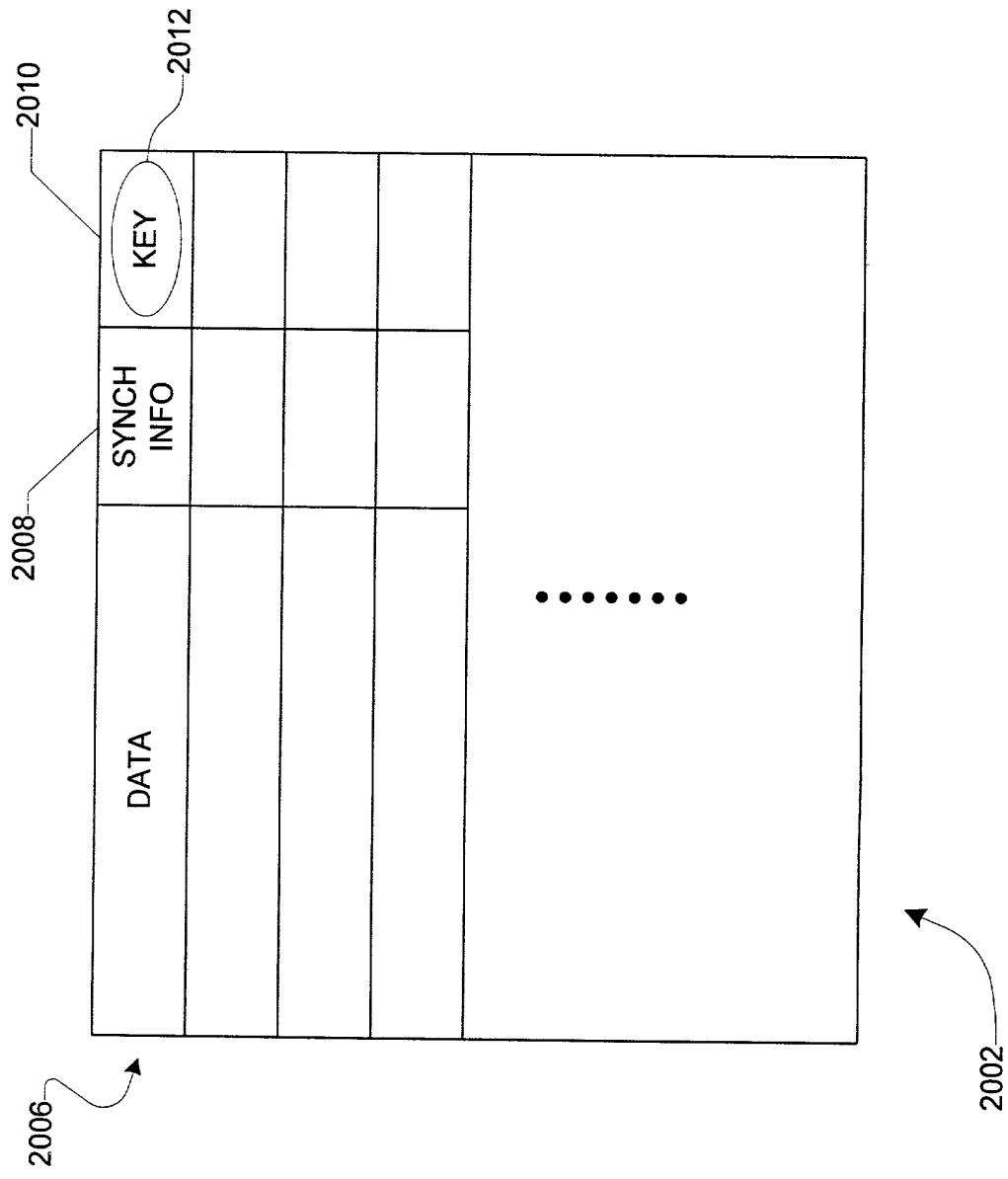


FIG. 20

Memory Access Control Table

ID	2106			2108		2110		2112	
	Base	Size	Access Key	Access Key Mask	Access Key	Access Key Mask	Access Key	Access Key Mask	Access Key Mask
0	Base	Size	Access Key	Access Key Mask	Access Key	Access Key Mask	Access Key	Access Key Mask	Access Key Mask
1	Base	Size	Access Key	Access Key Mask	Access Key	Access Key Mask	Access Key	Access Key Mask	Access Key Mask
2	Base	Size	Access Key	Access Key Mask	Access Key	Access Key Mask	Access Key	Access Key Mask	Access Key Mask
...									
63	Base	Size	Access Key	Access Key Mask	Access Key	Access Key Mask	Access Key	Access Key Mask	Access Key Mask

FIG. 21

APU issues DMA command 2202
DMAC looks up APU's key 2204
DMAC looks up memory access key 2206
DMAC compares APU key to access key 2208
MATCH? 2210
DMAC executes DMA command 2214
Error signal generated and access prevented 2212

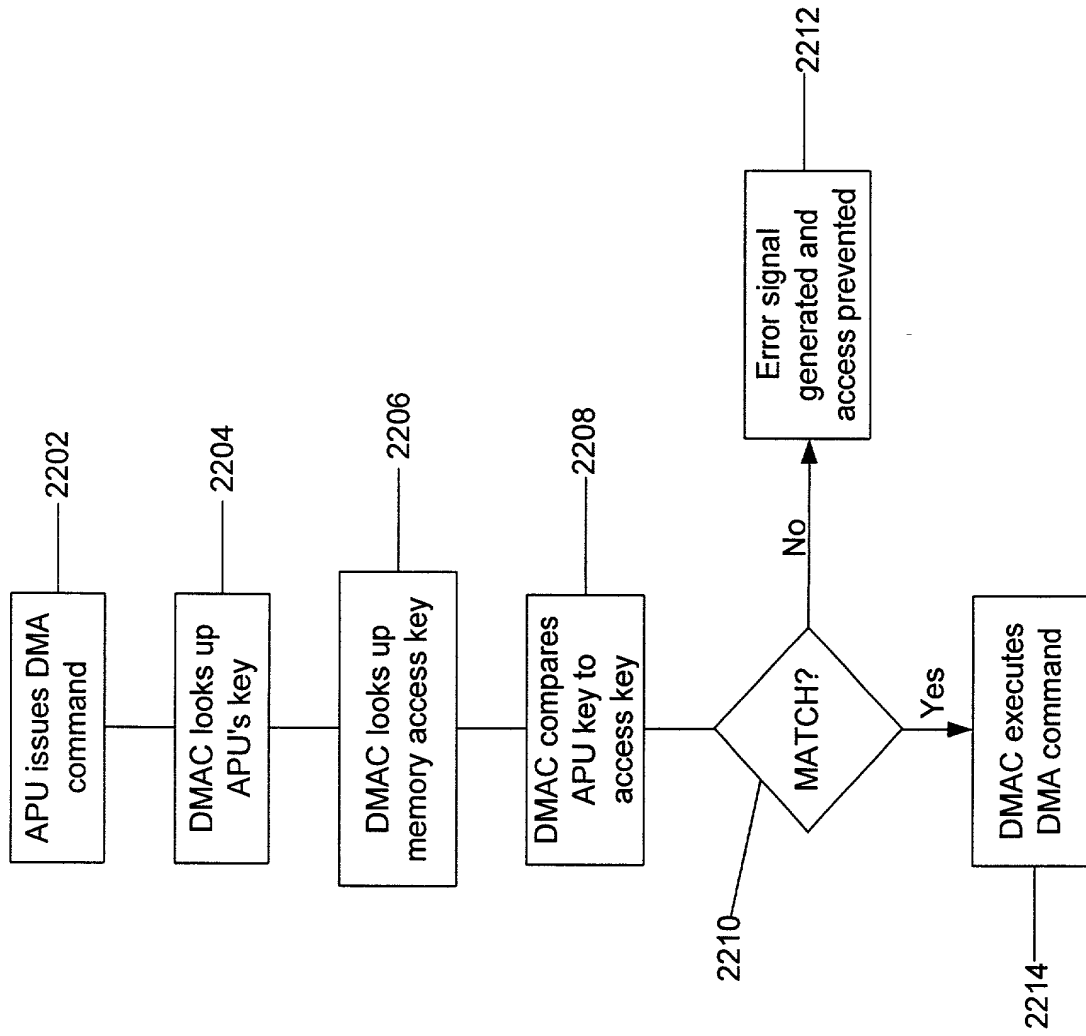


FIG. 22

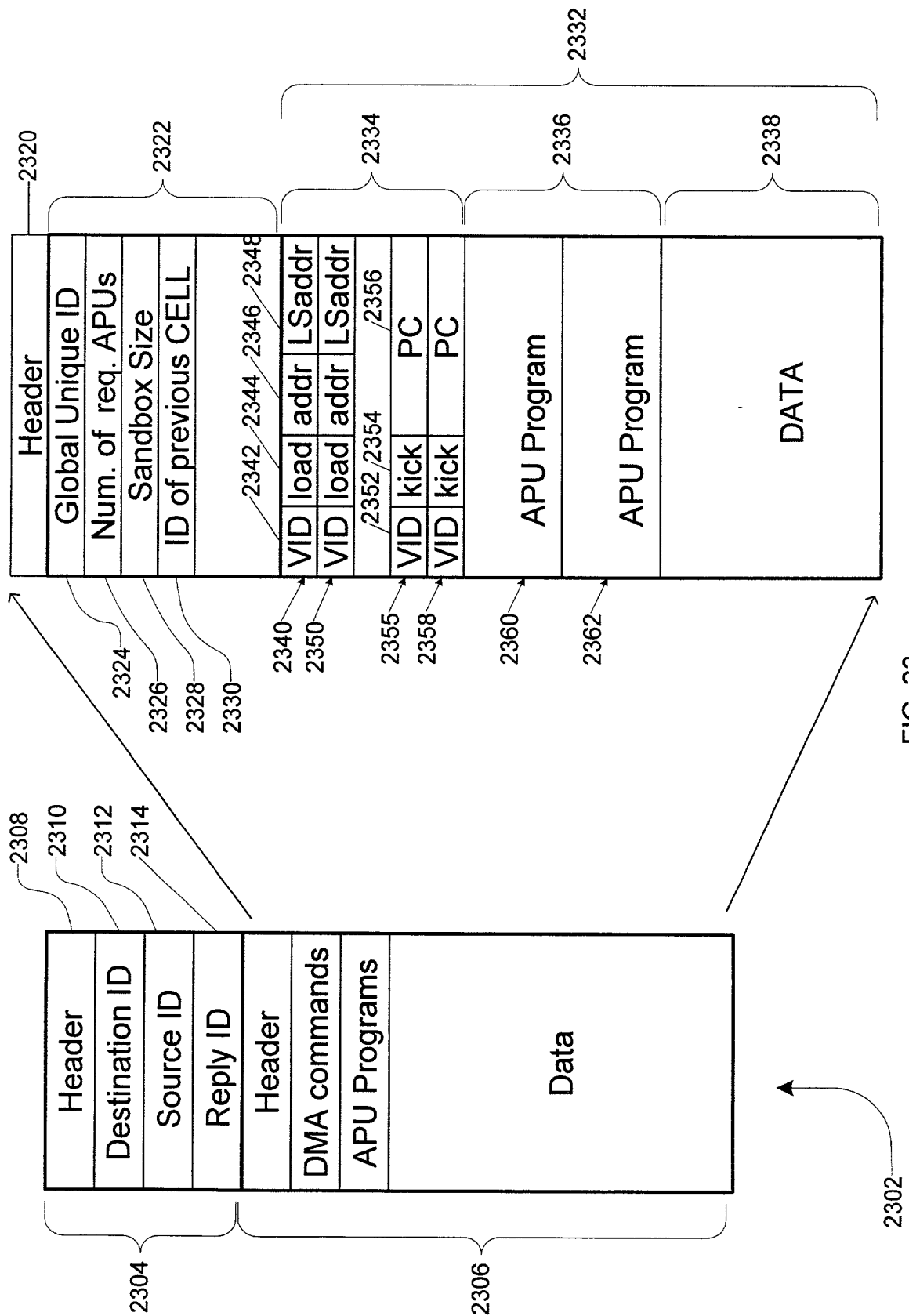


FIG. 23

FIG. 24 is a flowchart illustrating a process for executing an apulet. The process begins with an evaluation and designation of APUs (2410), followed by allocating DRAM memory (2412). The process then enables an interrupt request for the APU (2414) and issues a DMA command to load the apulet (2418). The apulet is then read from DRAM to local storage (2420), and the PU issues a DMA command to load the stack frame (2422). The stack frame is read from DRAM to local storage (2423), and the PU issues a DMA command to assign a key (2424). The DMAC updates the key control table (2426), and the PU issues a DMA command to start the apulet (2428). The apulet begins execution (2430), and the APU evaluates the stack frame (2432). The APU issues multiple DMA commands to load data in local storage (2434), and data is read from DRAM to local storage (2436). The APU processes the apulet and provides a result (2438), and the APU issues a DMA command to store the result in DRAM (2440). The result is written from local storage to DRAM (2442), and the APU issues an interrupt request to the PU (2444).

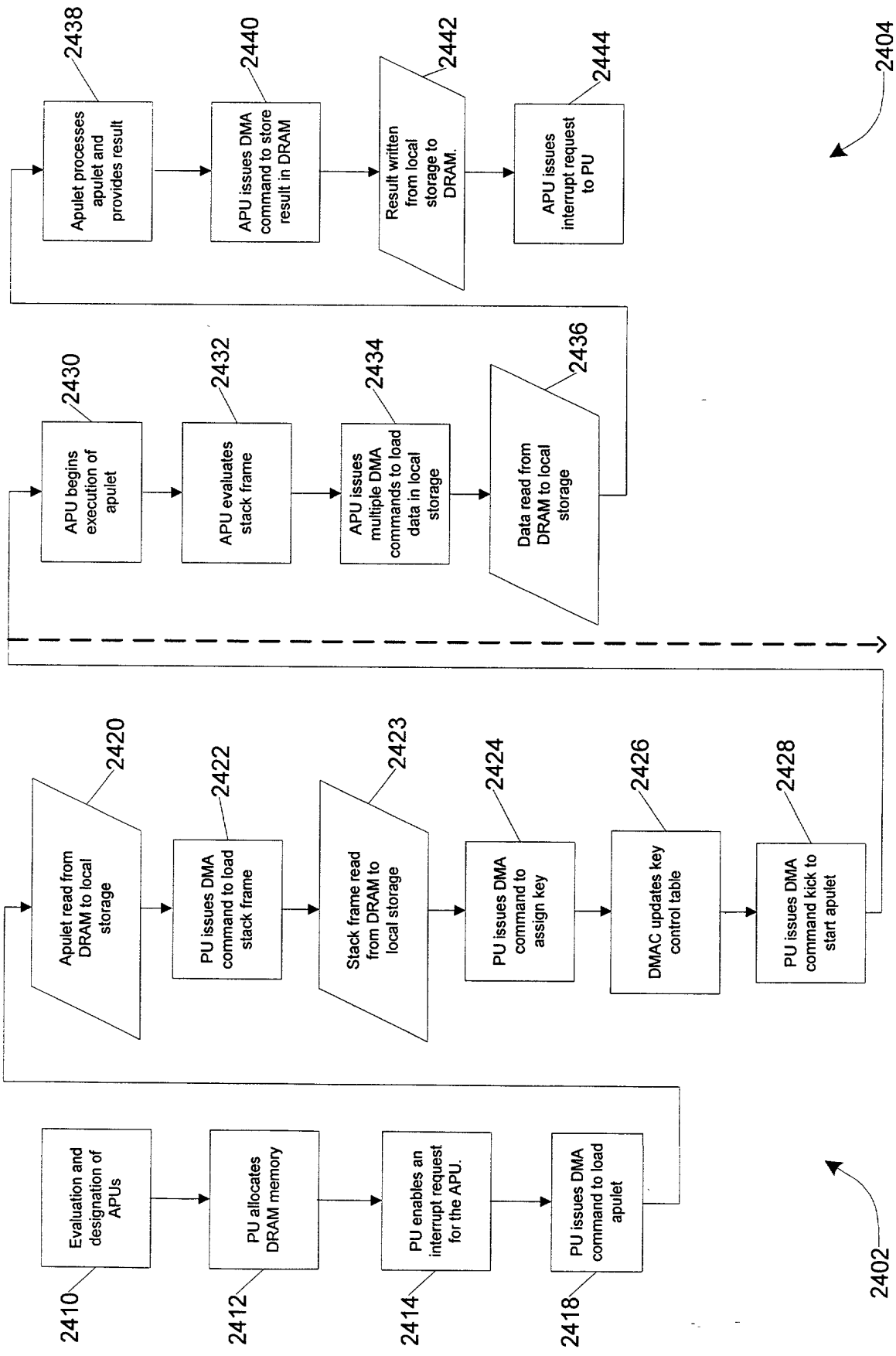


FIG. 24

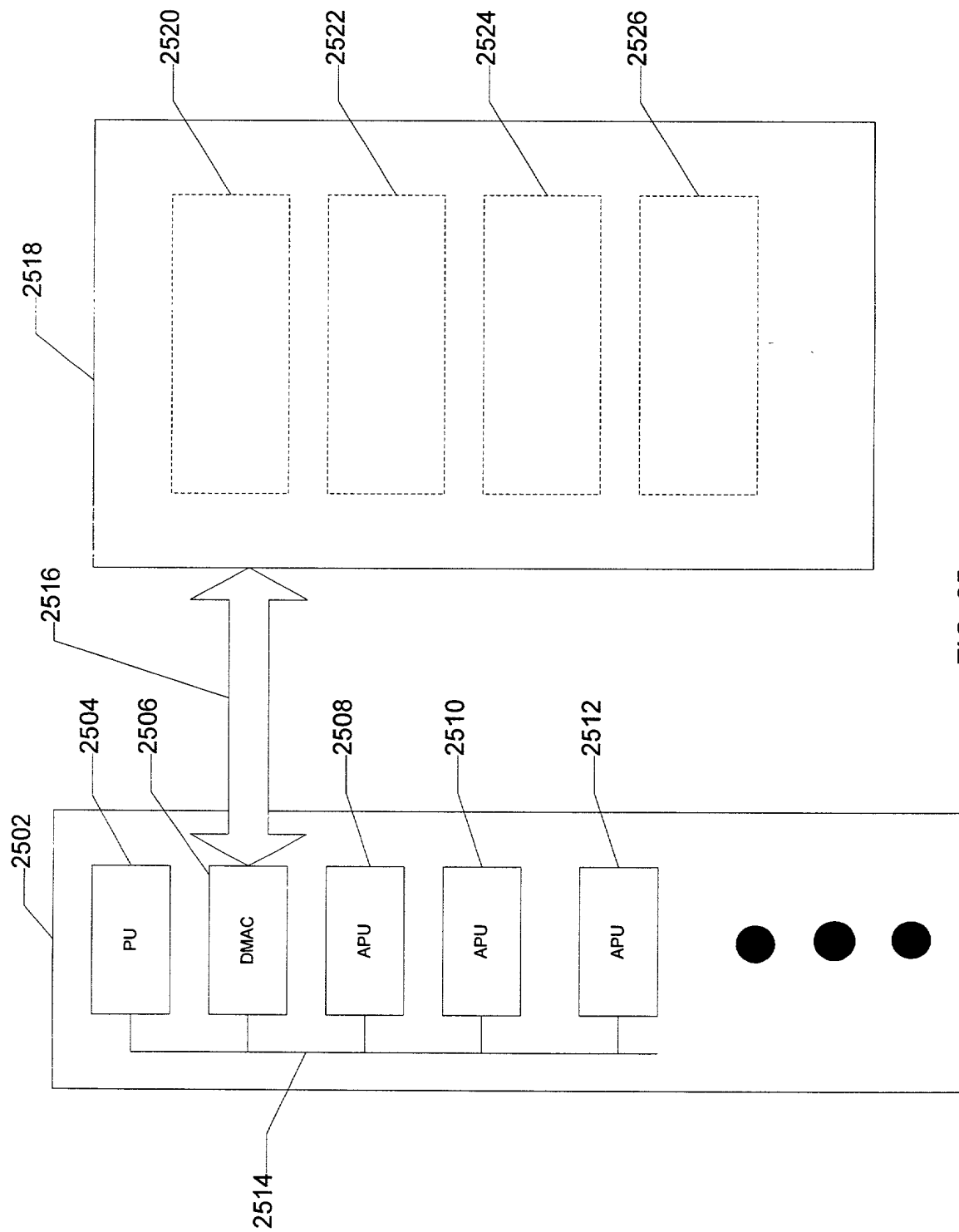


FIG. 25

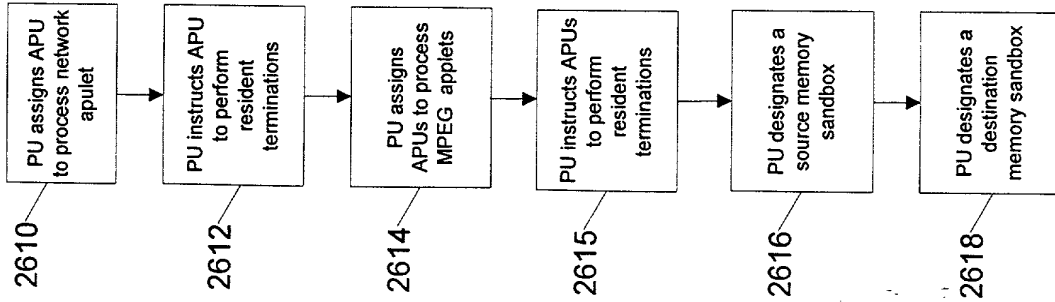


FIG. 26A

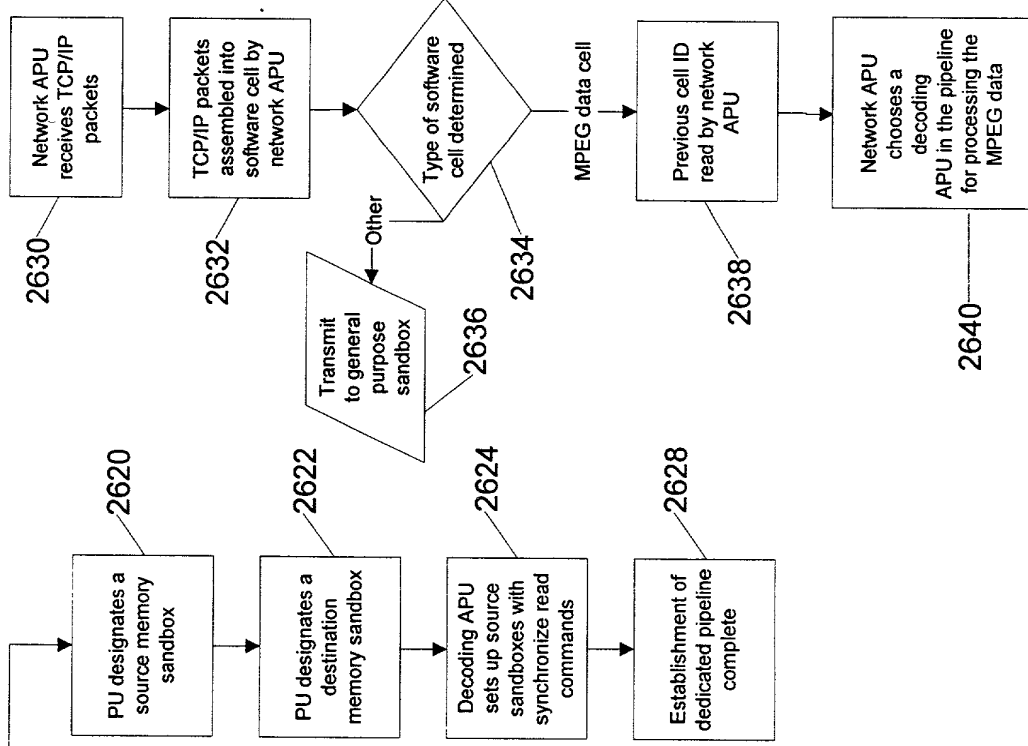


FIG. 26B

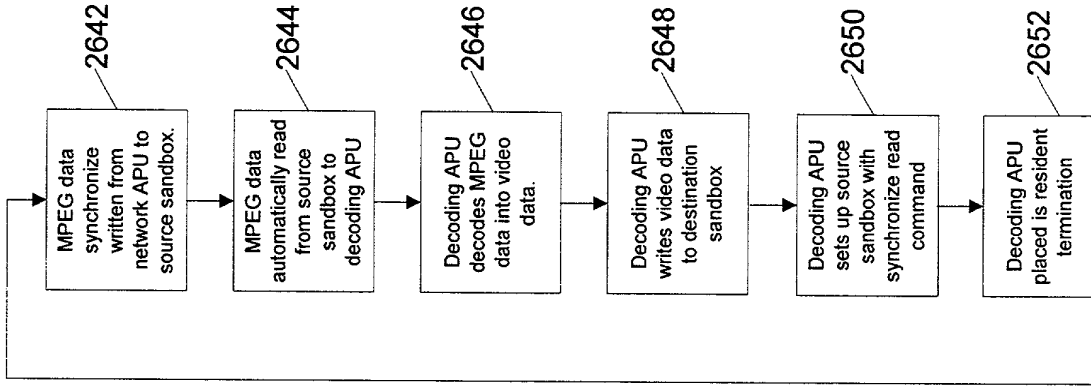


FIG. 27 is a block diagram of a system architecture for rendering 3D objects. The system includes a 3D object (2704) and a 3D object (2710) and a 3D object (2716). Each 3D object is associated with a Sandbox (source) and a Sandbox (destination). The Sandbox (source) is connected to a 3D object. The Sandbox (destination) is connected to a Display list. The Display list is connected to an APU (2702). The APU (2702) is connected to a Rendering Engine (2720). The APU (2702) is also connected to a 3D object (2710) and a 3D object (2716). The 3D object (2710) is connected to a Sandbox (source) and a Sandbox (destination). The Sandbox (source) is connected to a 3D object. The Sandbox (destination) is connected to a Display list. The Display list is connected to an APU (2708). The APU (2708) is connected to a Rendering Engine (2720). The APU (2708) is also connected to a 3D object (2716) and a 3D object (2710). The 3D object (2716) is connected to a Sandbox (source) and a Sandbox (destination). The Sandbox (source) is connected to a 3D object. The Sandbox (destination) is connected to a Display list. The Display list is connected to an APU (2714). The APU (2714) is connected to a Rendering Engine (2720). The APU (2714) is also connected to a 3D object (2710) and a 3D object (2716).

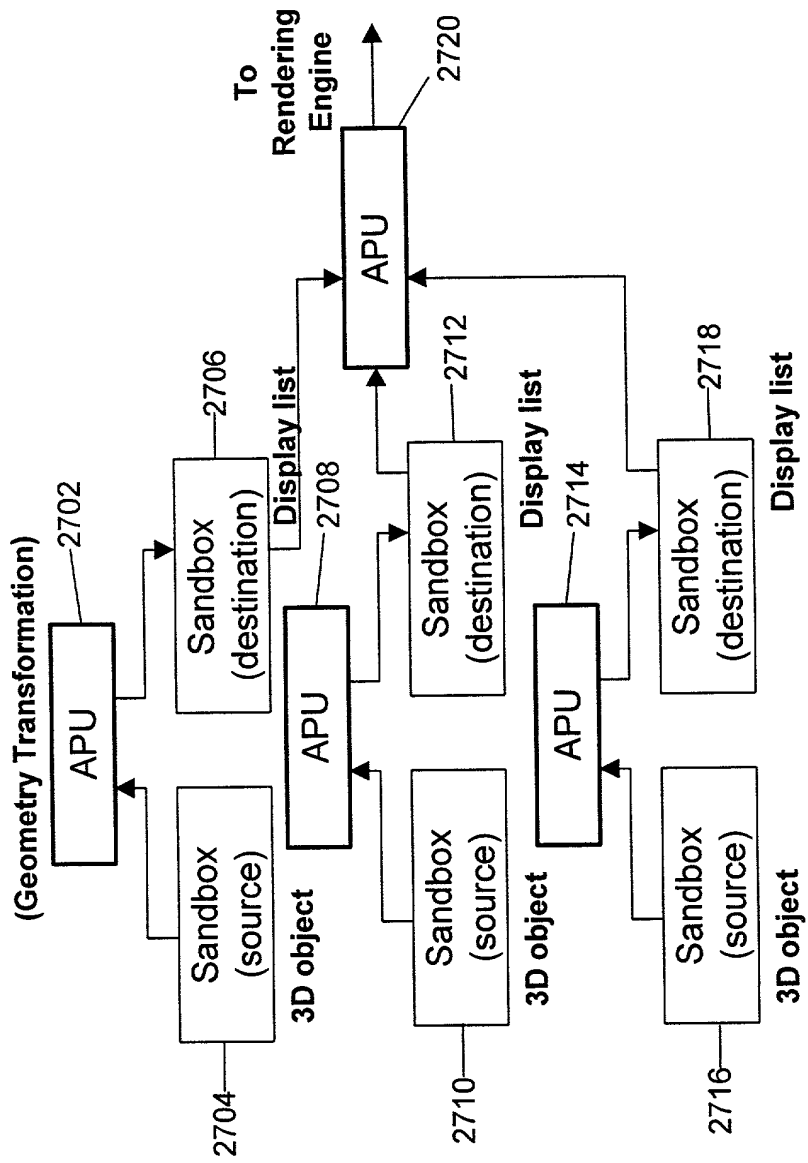


FIG. 27

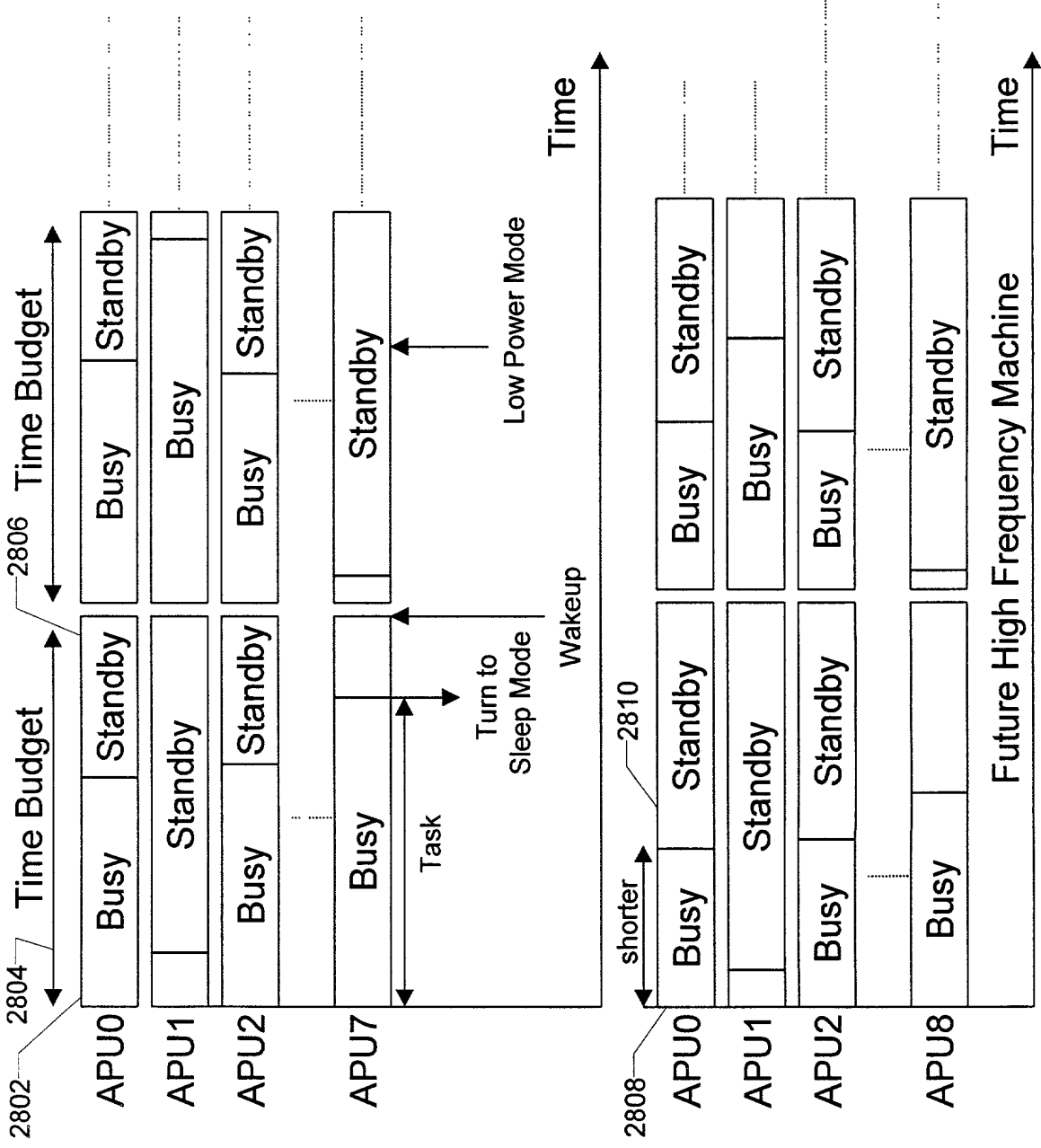


FIG. 28